Challenges in the Gate Stack Technology for Future Semiconductor Devices

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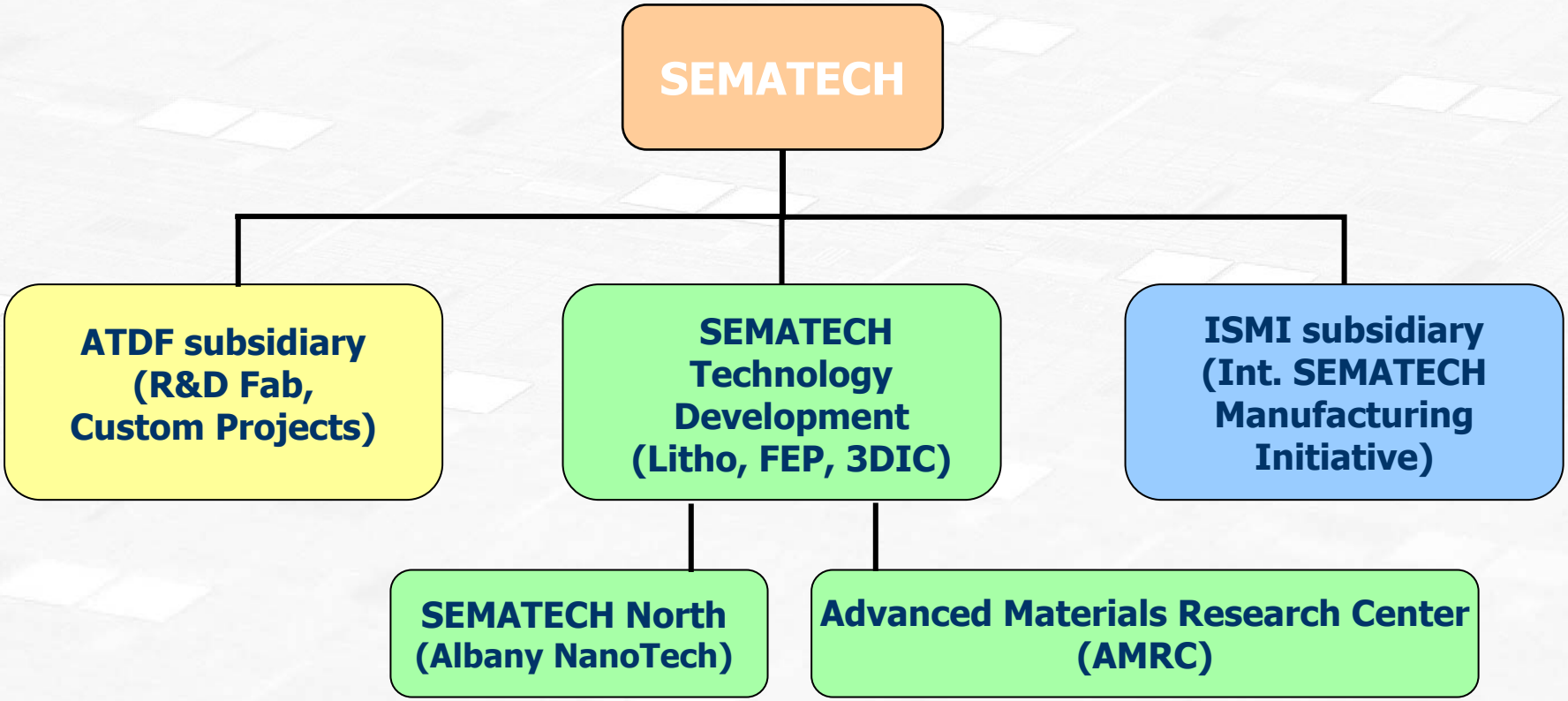
Advanced Gate Stack Program
METS-ECR Program

Accelerating the next technology revolution.

Outline

- Intro. to SEMATECH, FEP division
- Future CMOS technology
- Review of Alt. Gate Stack Research
  - Case 1: Intrinsic problem of high-k dielectric
  - Case 2: Poly silicon gate vs metal gate
  - Case 3: EWF measurement
  - Case 4: Fermi level pinning – a misnomer?
- Summary

The SEMATECH Family



SEMATECH FEP program

- **Advanced Gate Stack**
  - Metal/high-k gate stack for Si and high transport substrate (HTS)
  - Dual workfunction metal gate CMOS baseline
- **Memory program**
  - DRAM memory dielectric, Flash (CTF, QD)
  - Novel memory devices and materials (ReRAM, CBRAM, molecular)
  - Future SRAM technologies
- **CMOS Scaling Technology**
  - High transport substrate (HTS) process: Ge, III-V MOSFET
  - Low resistance extension/contact technology
  - Non-planar device technology (FinFET, Silicon nanowire …)
- **Electrical characterization**
  - Reliability WG for advanced gate stack devices
  - Advanced Test Technology center: Test methodology for future devices
- **Future areas of interest in planning stage**
  - CMOS compatible MEMS sensors
  - Solar cell technology
  - Design for manufacturing (DFM)

Core Tools and Process Capability

ECR

WLR auto probe station w. 30MHz pulse capability (B)

Semi-auto dev. probe Station w hot chuck

Manual station w ultra short pulsed I-V measurement

UHF CV, DCIV, Charge pumping

Cryogenic probe station with RF capability (2") (4K-425K)

Advanced Dielectrics

ALD HfO2, HfSiO (B)

ANELVA DC/RF PVD high-k (B)

TEL SPA PNO(8")

VESTA plasma anneal (B, 07/05)

AMAT RTA, VESTA RTO/RTA,

Excelis spike anneal

Advanced Electrode

ANELVA low damage metal PVD (B)

AVIZA ALD Metal (B)

VESTA PEALD metal (B, 04/05)

PSMC High pressure H2/D2/O2 anneal

Basic Process/CMOS Scaling

CMOS baseline (Lgate=30nm, 85nm)

Metal etcher (RT/ HT chamber)

Flash anneal

Epi-Si, SiGe. Ge Silicides/Germanides

RingFET flow
Capacitor flow
MIM capacitor flow
Charge separation structure flow
Rep. gate flow
Dual metal/dual high-k flow
FinFET device flow

Metal Wet Etch

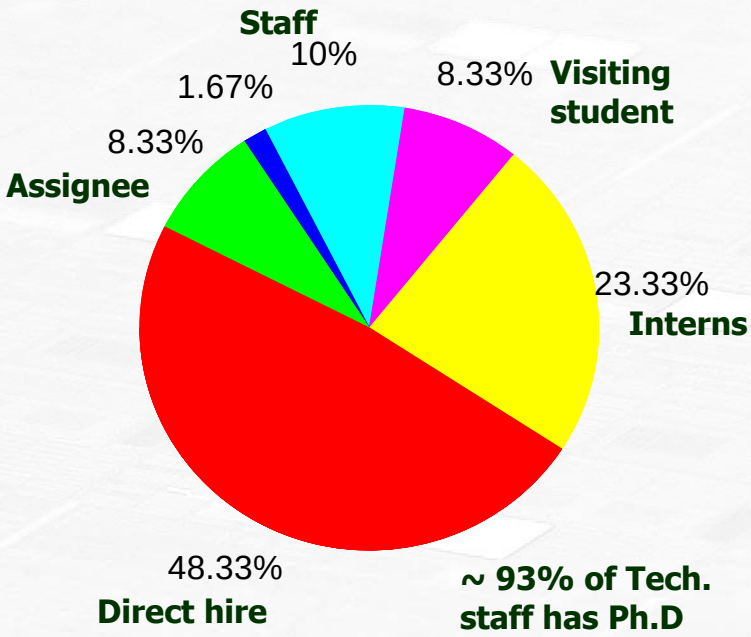
Selective hi-k etch

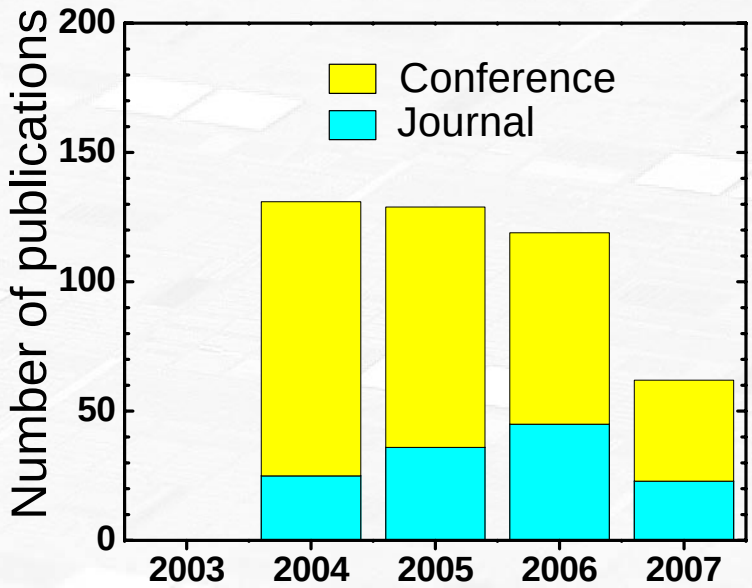
Backside etch

- Metrology group (XRR, GA XRD, Quantox, SE, TXRF, AR XPS); Micro-Raman, QMSA, CBED, IPE
- Test lab (4 semiauto prober), PCL Lab (2 TEMs+EELS, SIMS),
- 200mm poly/ox baseline(STI, ISSG oxide, 85nm Lpoly, NiSi, $CoSi_2$, W plug, Al metal)

+ 80% of toolset is 300 mm or bridge

Strong collaborations with university





- Visiting students/Interns from 10 universities are currently working with FEP team (CNNU, POSTECH, Texas Tech., SKKU, Stanford, UCB, UFL, UT Austin, UT Dallas, Yale).
- FEP works with more than 50 universities on sponsored research projects, jointly funded projects and third party funded projects.
- 30% of FEP publication is joint publications with the collaboration partners

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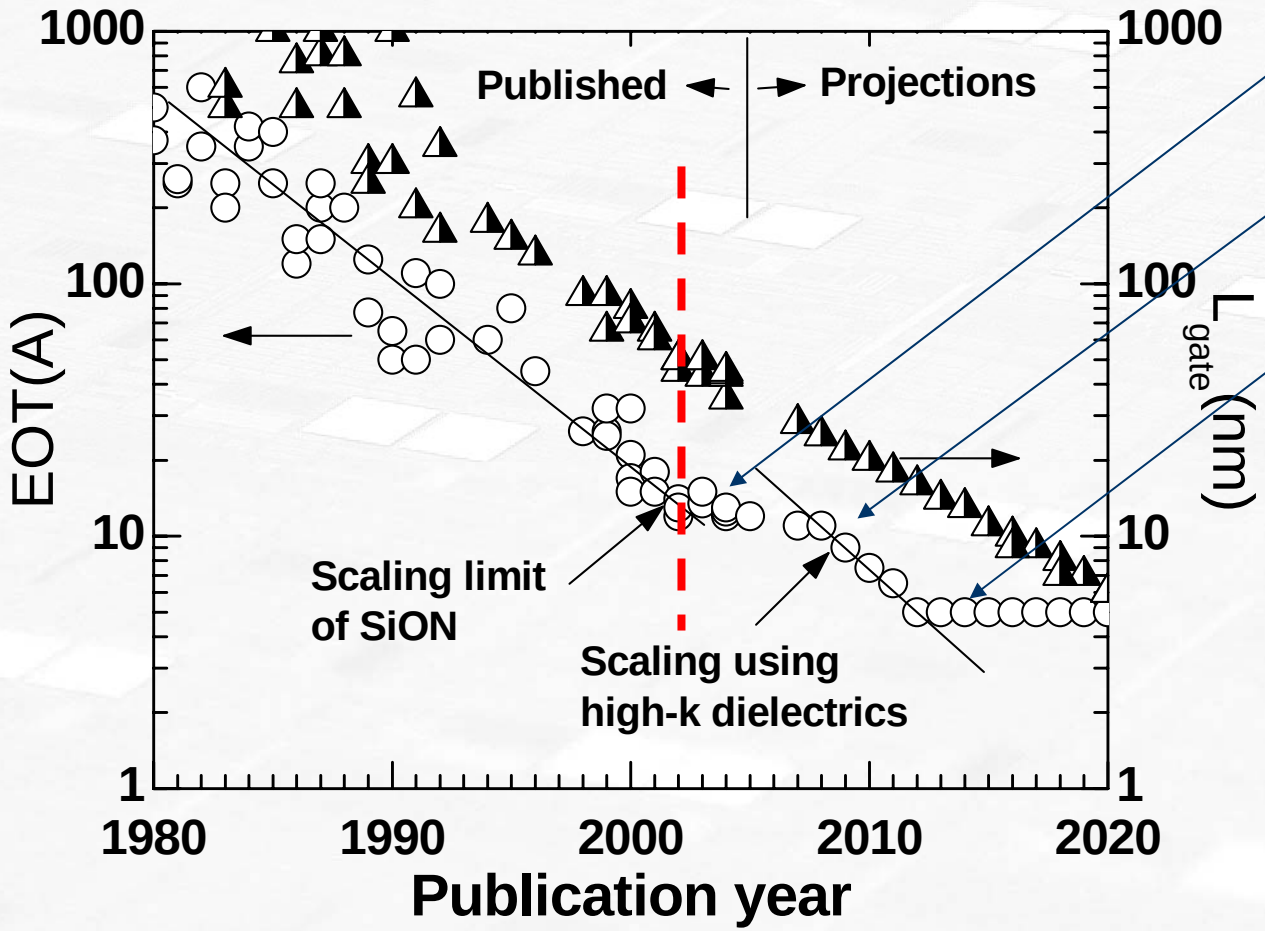
Evolution of CMOS technology

Tech. Node	Litho	~L_{Poly}	Key FEOL technology innovations
.5um	i-line	250nm	LOCOS, Salicide
.35um	i-line	180nm	Low Doped Drain (LDD):
.25um	i-line	135nm	LOCOS/ STI, Silicon on Insulator (SOI):
.18um	248nm	90nm	RTNO
.13um	248nm	~ 65nm	Offset Spacers, Cu BEOL
90nm	193nm	~ 45nm	Strain Engineering, Heavily nitrided oxide
65nm	193nm	~ 35nm	More aggressive stress Engineering, **End of oxide scaling**
45nm	193nm i	~ 20nm	Device customization, Metal/high-k
32nm	193nm i	TBD	Physical scaling
22nm	EUV	TBD	Alternative channel or Novel devices (planar or non-planar)

Scaling of SiO_2 based gate oxide is OVER in 2002 Yet, it took 3-4 more years to recognize it.



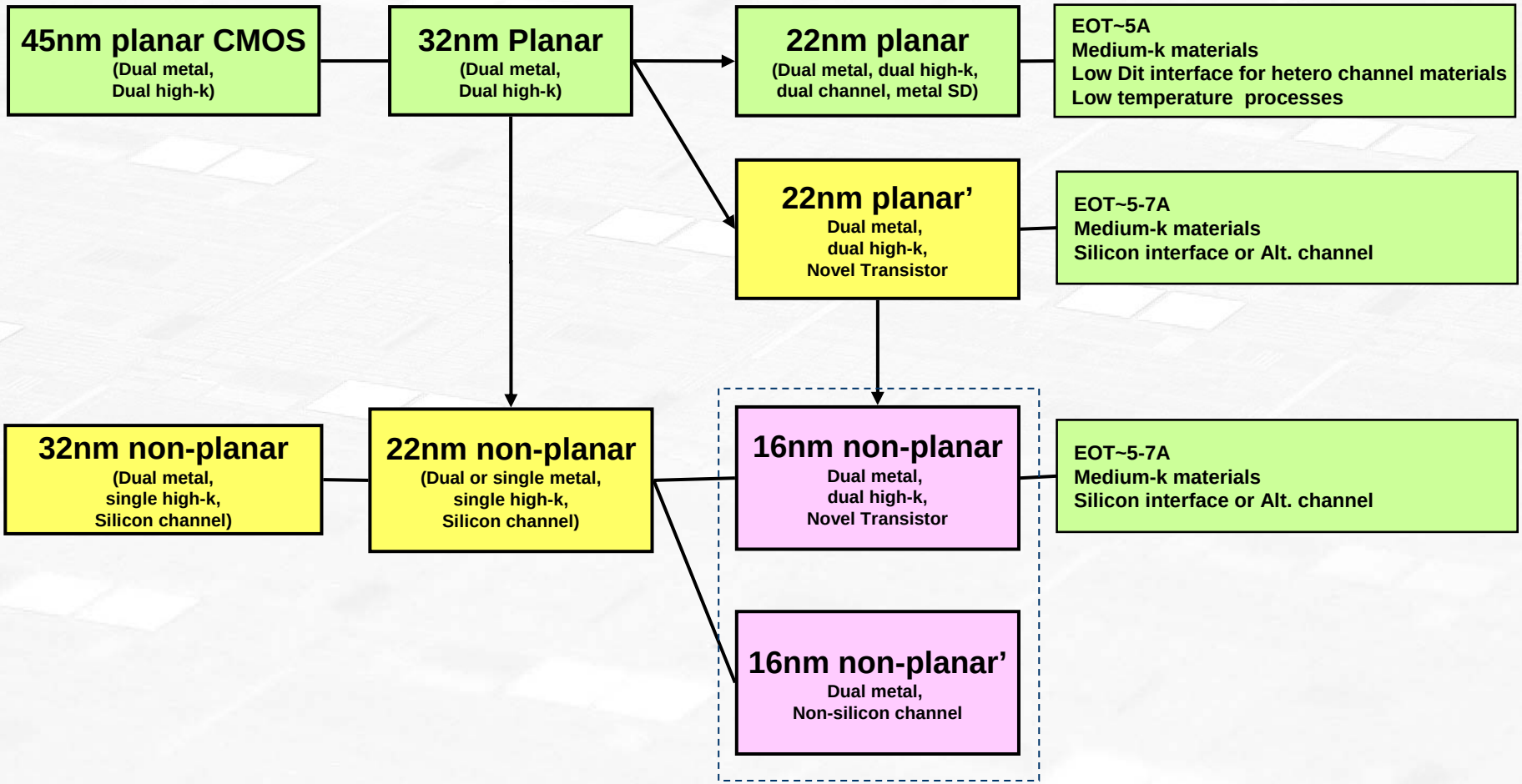
Oops?

High-k can do it!

After my retirement

Can Metal/high-k gate stack save the scaling problem?
Do we still need the physical scaling ?

Future CMOS technologies



- 32nm node technology can be a scaled version of 45nm node
- No clear direction towards 22nm node technology yet.
- In any case, the challenge beyond 32nm is paramount.

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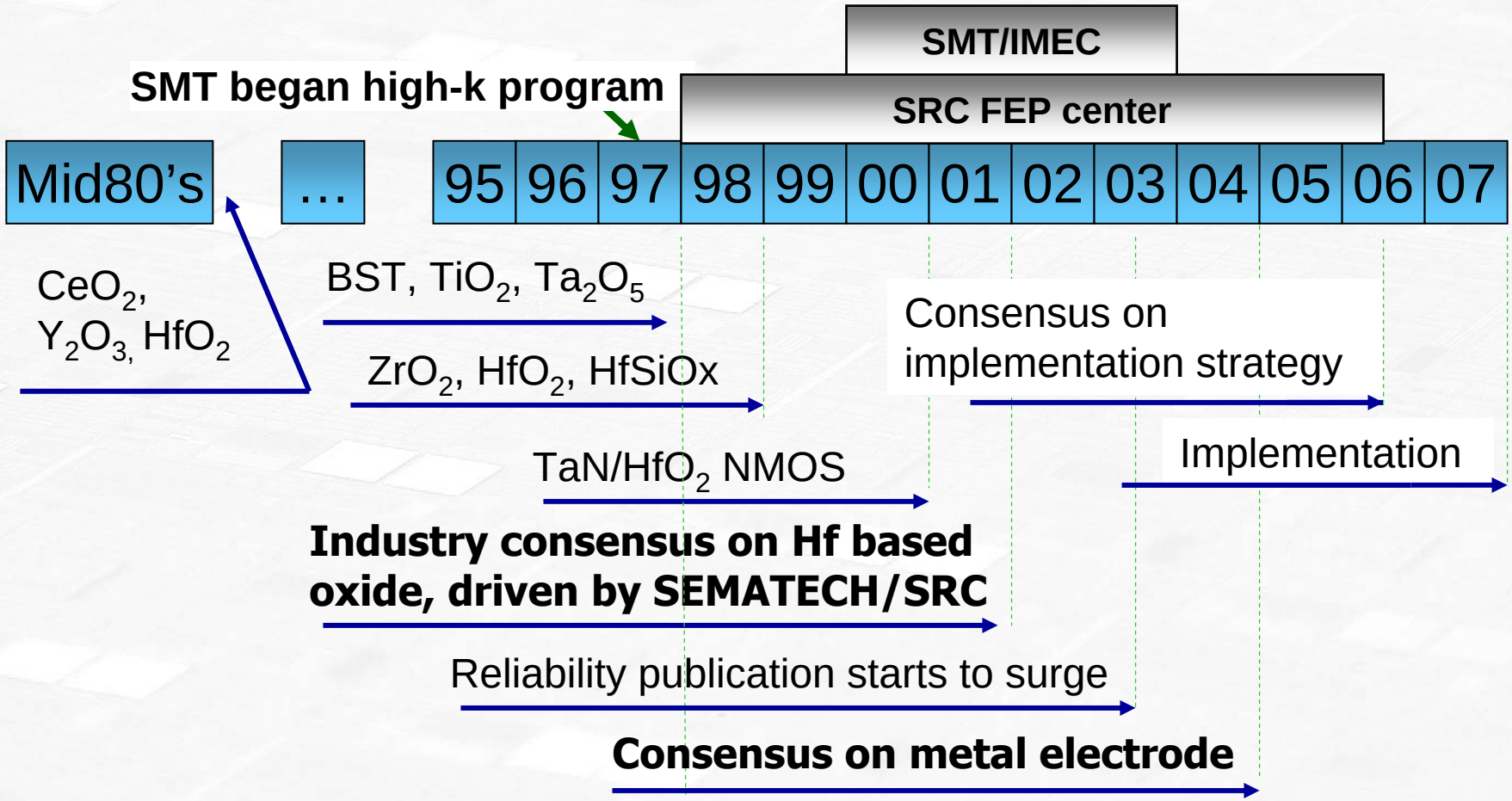
History of high-k dielectric research



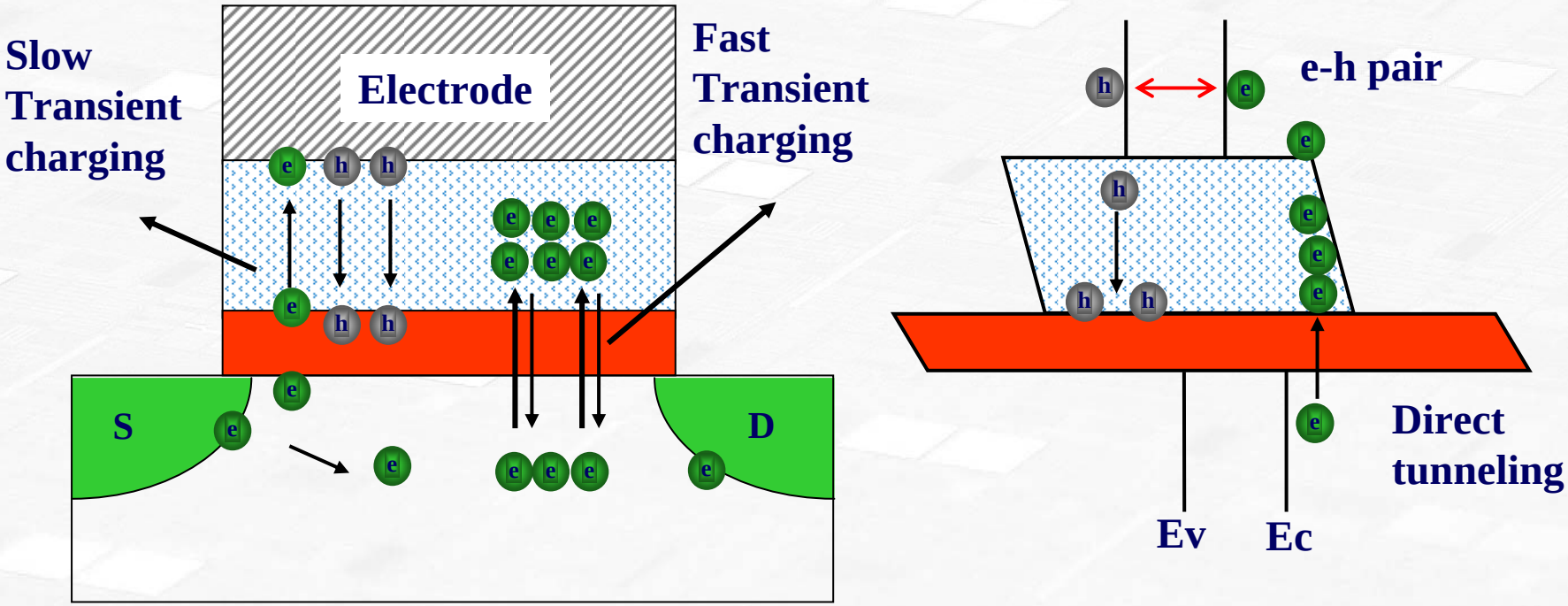
- Gate stack research is an example of well organized R&D activity
- Major decisions were made through the group activities
- Yet, there are many aspects that could have been handled better

Case 1: high-k dielectric – intrinsically worse than SiO_2

- High-k dielectrics (HfO_2, Y_2O_3, Al_2O_3) */ M.Balog, TSF, 1977, L.Machanta, EDL, 1988,*
- First order material screening through thermal stability */ T.J.Hubbard and D.G.Schlom, JMS, 1996*
- Selection of HfO_2 */ Y.Jeon et al., IEDM, 1999, G.D.Wilk et al., APL 1999*
- Proof of scalability using nitrided interface */ R.Choi et al., VLSI 2001*
- Remote phonon scattering */M.Fischetti et al., JAP, 2001*
- HfO_2 on Ge MOSFET / C.Chui et al., IEDM2002
- Single pulse characterization */A.Kerber et al., EDL 2003*
- Correction of mobility calculation */ W,Chu et al., TED 2004*
- FTCE using ultrashort pulse characterization */ B.H.Lee et al., SSDM 2004*
- Mobility matched with SiON at EOT=1nm */ M. Quevedo et al, IEDM 2005*

Above papers are listed as an example only

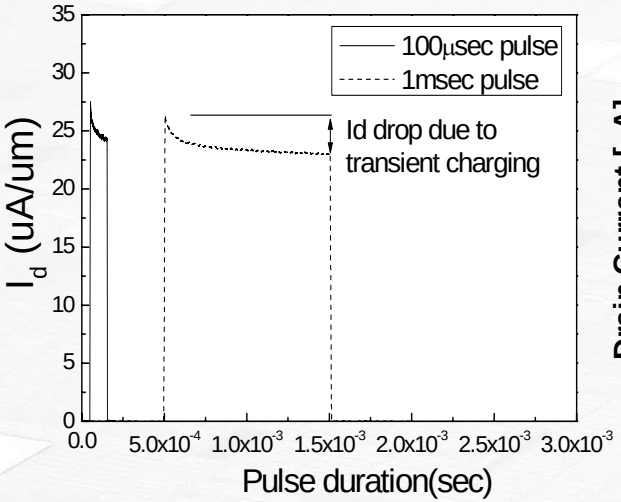
What is Fast Transient Charging Effects (FTCE)?

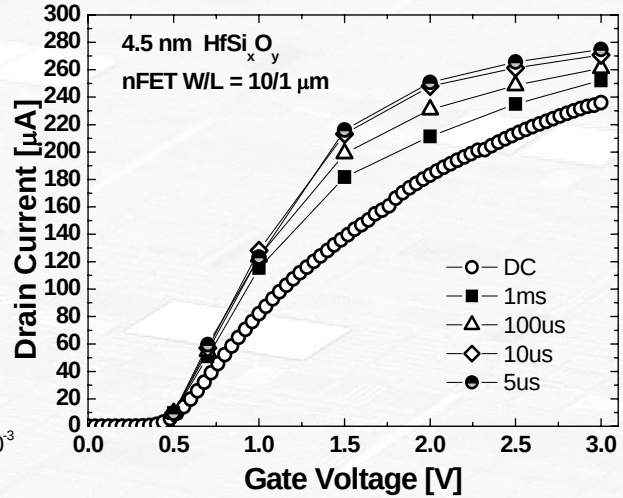


- TCE is a working model referring overall effects of the charge exchange between channel and high-k layer.
- Small bandgap and thin interfacial layer enhance TCE.

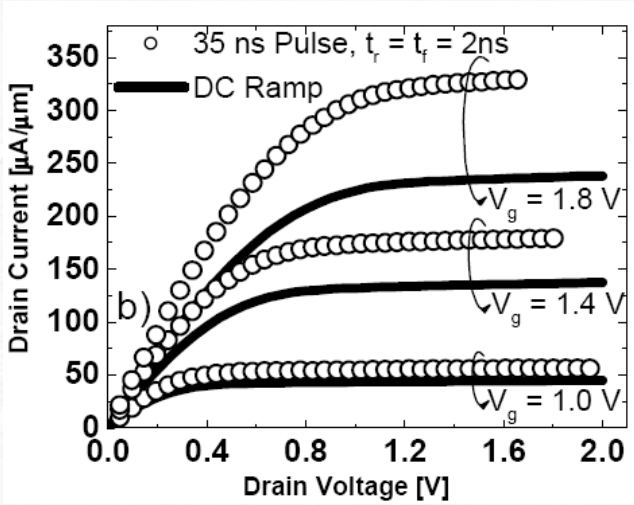
B.H.Lee et al.IRPS, 2004

Performance enhancement with pulsed I-V

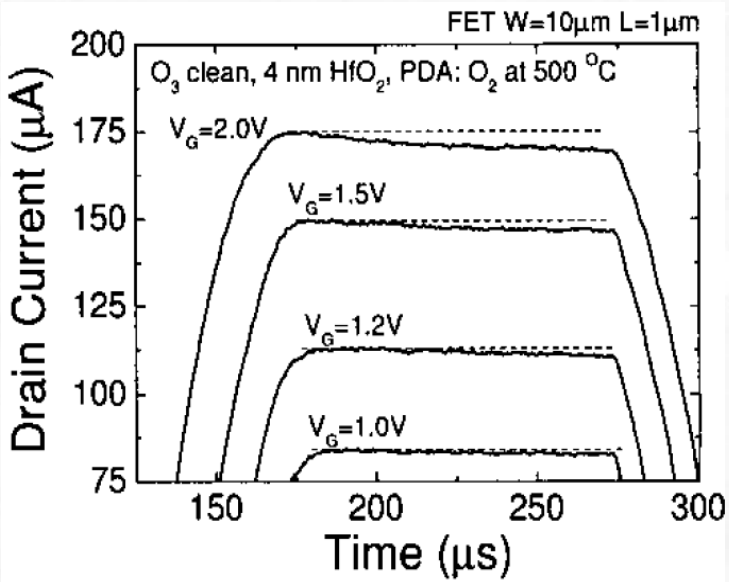




B.H.Lee et al., SSDM, 2004



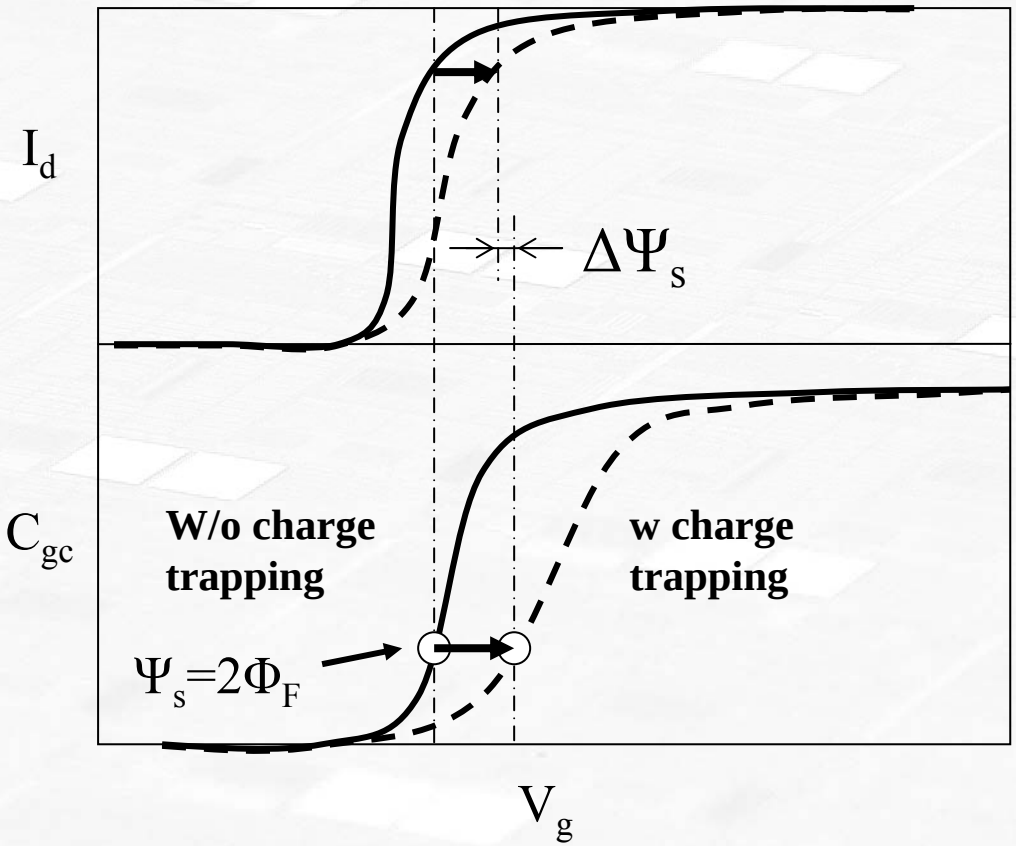
C.Young et al., SSDM, 2004



A.Kerber et al., IRPS, 2003

- Conventional DC measurement underestimates the intrinsic current drivability of high-k device due to concurrent electron charging.
- Direction of process development should be changed to reduce the bulk trapping

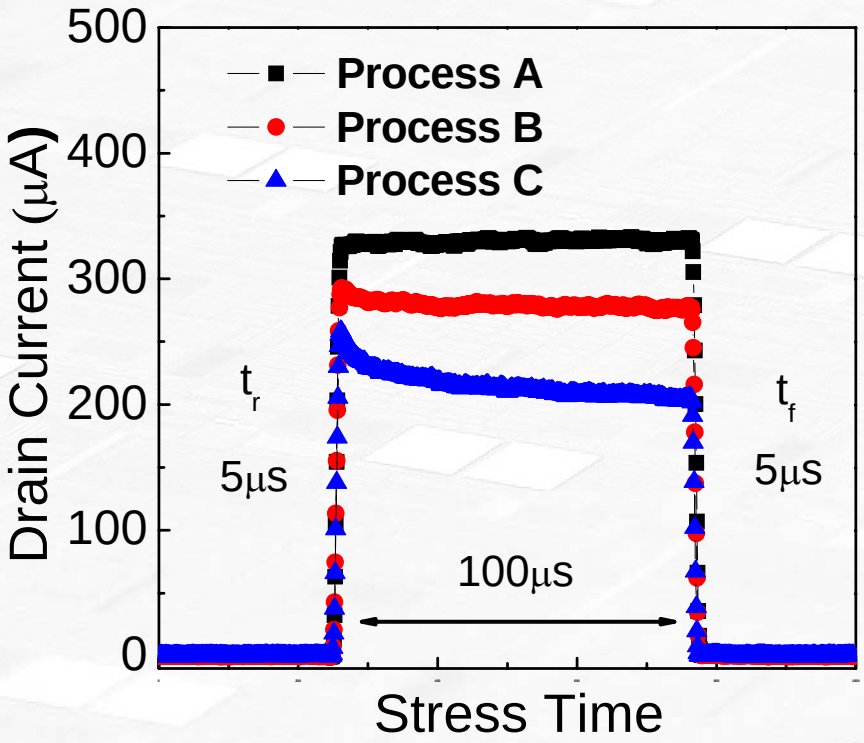
Transient charging slews CV and I_d-V_g curves

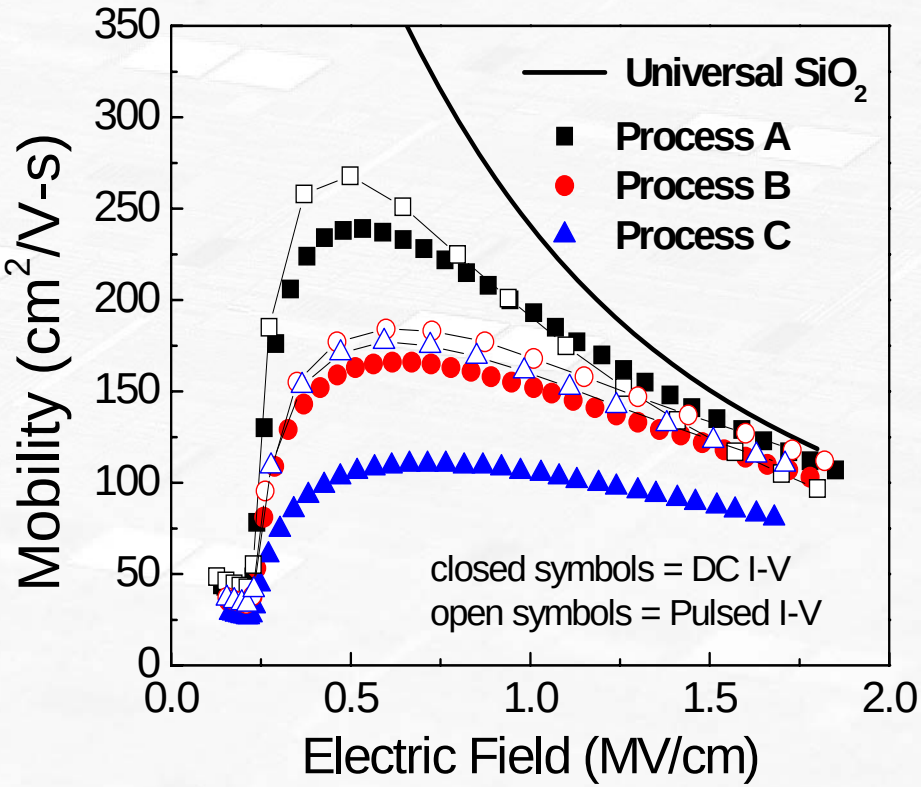


- Charge trapping induced CV and I_d-V_g curve slews are not always matching.

B.H.Lee et al., ISTC, 2005

Transient charging induced mobility skew

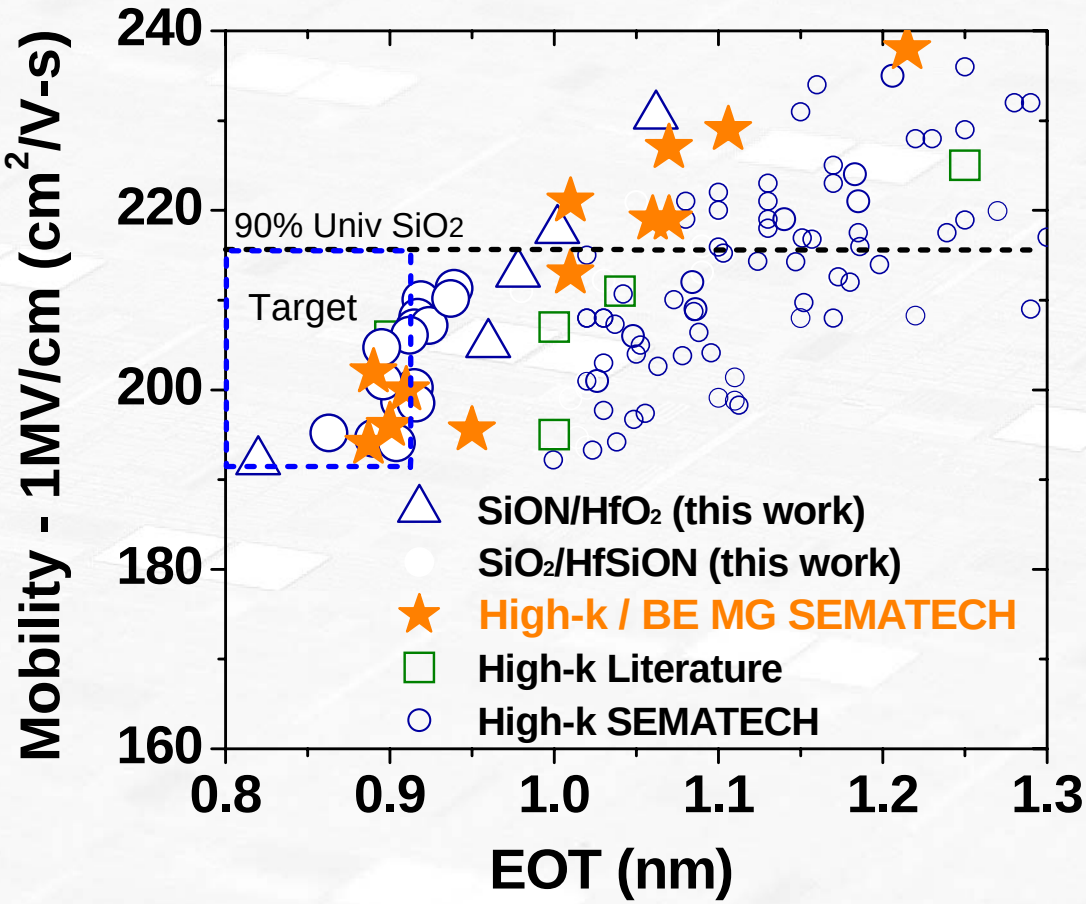




- Transient changing is abruptly reduced between process A,B,C.
- Once transient charging is eliminated, remaining mobility degradation is not as significant as many of us thought before.

J.Sim et al., INFOS, 2005

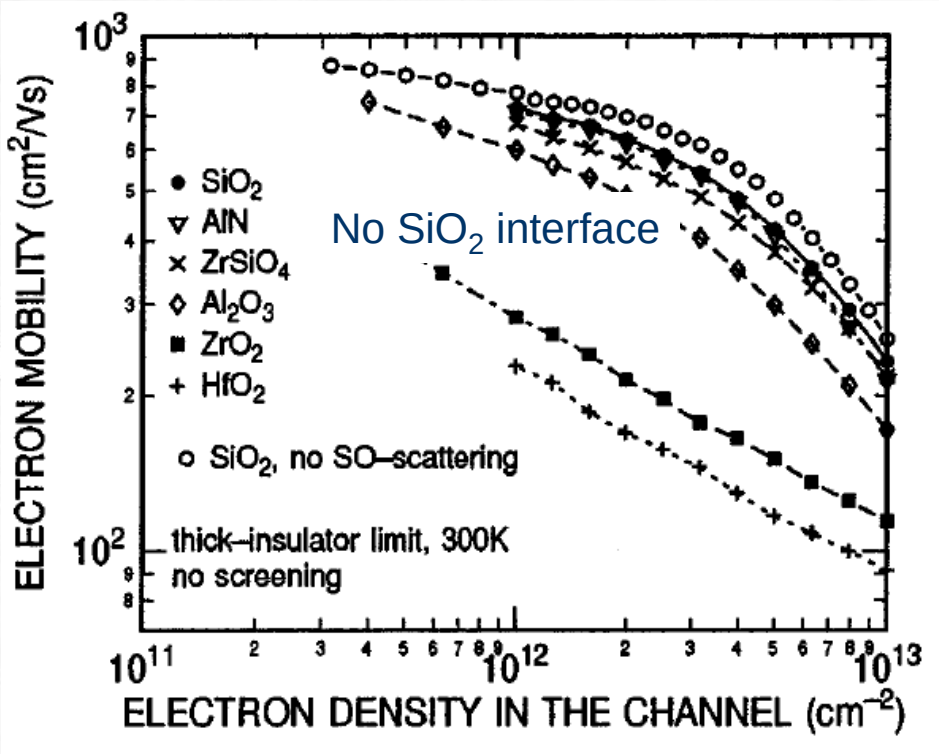
Mobility values demonstrated at sub. 1nm EOT



- Mobility of high-k dielectric can be matched with SiON at ~1nm EOT.
- ~0.8nm EOT, the mobility of high-k device is still in competitive range.
- More innovative solution is needed for the EOT regime below 0.7nm.
- New channel materials might be used to explore no interface option.

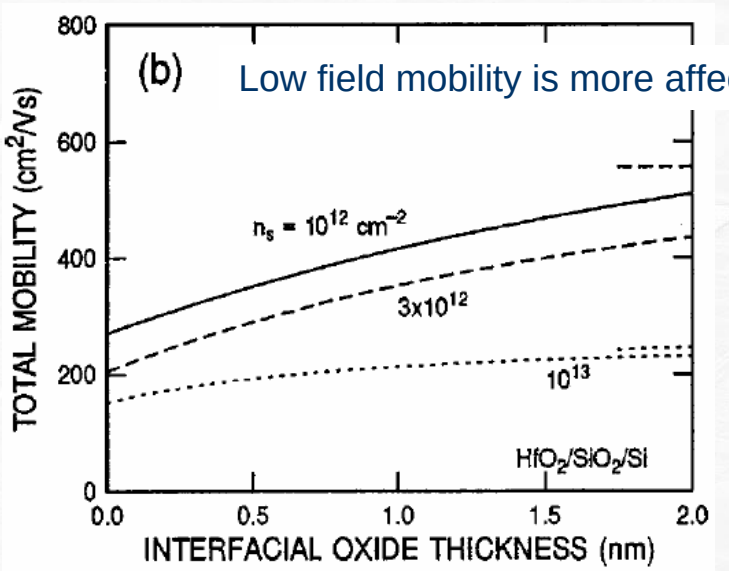
- S.Krishinan et al., Performance Enhancement of pMOSFETs with Optimized **HfO_2/TiN Gate Stack on Si(110) Substrates**, IEDM 2006.

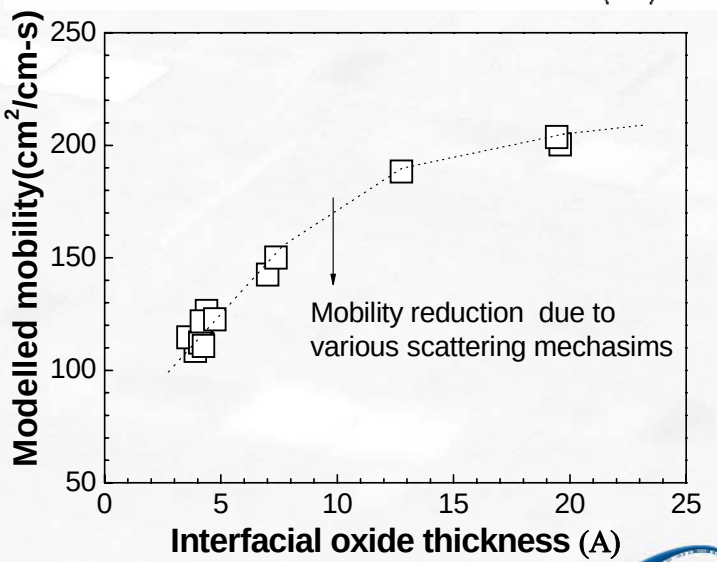
Scaling of interfacial oxide is limited by various scattering mechanisms



M.Fischetti et al., JAP, 2001.

- Scaling of interfacial oxide or elimination is not a good option of Si-channel devices.





J. Ghavartin et al., ISAGST 2004.

Case 1: high-k dielectric – intrinsically worse than SiO_2

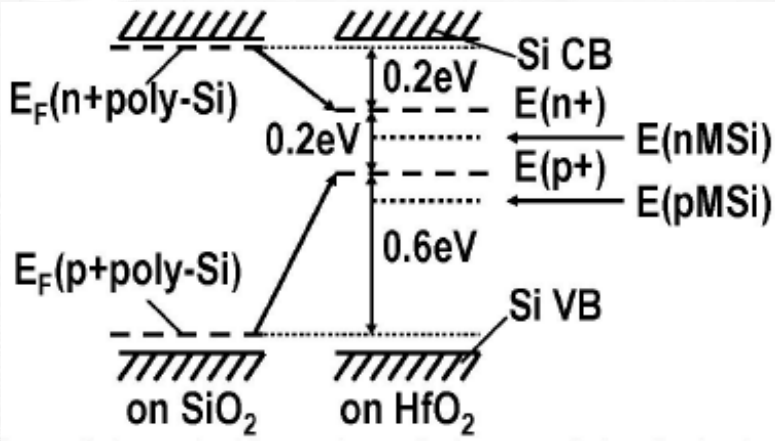
- Excellent starting point to sort out high-k dielectric candidates: Study on thermal stability
- Why it took 6 years to find thinning of HfO_2 is enough to recover the mobility?
  - Fear to challenge the physics of phonon scattering
  - Try to achieve unnecessarily low leakage current, unclear target
  - Didn't question the validity of test methods and tools we've been using for SiO_2.
- Take home lesson
  - Need to define the goal clearly (Why and When the results will be needed) and study the physical mechanisms at target range.
  - Find a way to isolate the intrinsic problems from extrinsic problems.
  - New materials require new tools…

Case 2: Polysilicon gate vs Metal gate

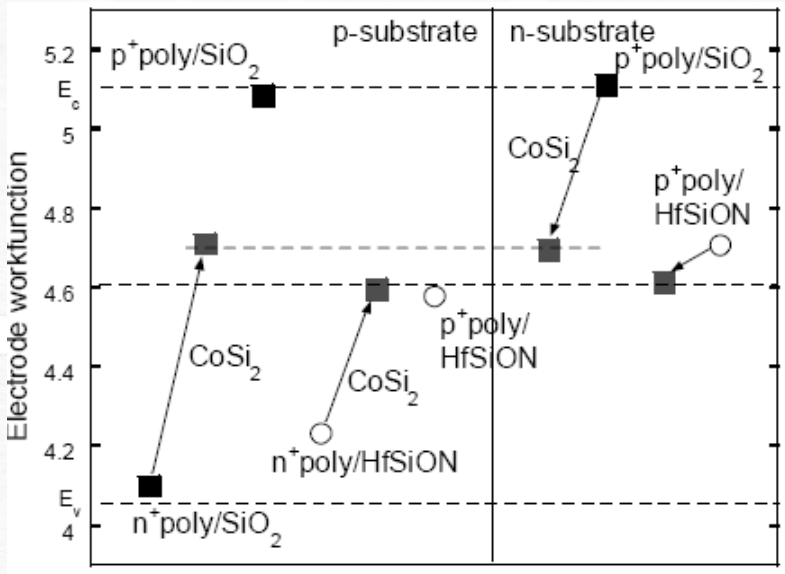
- First replacement gate MOSFET */ A. Chatterjee et al., IEDM, 1997*
- **TaN gate MOSFET with EOT<1nm** */B.H.Lee et al., IEDM 2000.*
- **EWF shift due to Al dipole at poly/HfO_2 interface***/ J.H.Lee et al., IEDM 2000*
- Fully silicide gate / B.Tavel et al., IEDM 2001
- Fermi level pinning at metal/high-k interface */ Y.Yeo et al, VLSI 2001*
- EWF control of NiSi FUSI gate / J.Kedzierski et al. IEDM 2002
- Fermi level pinning at polysilicon/HfO_2 interface */ C.C. Hobbs et al., IEDM 2003, TED 2004*
- Working nMOS/pMOS metal/high-k device */ R.Chau et al, EDL 2004*
- Influence of oxygen vacancy on EWF of Pt */ E.Carier et al., VLSI 2005*
- **Dual Metal/ Dual High-k CMOS** */ Z.Zhang et al., VLSI, 2005*
- La induced interface-dipole model */A.Toriumi's group, SSDM 2006*
- **Metal gate induced strain effect** */ C.Y.Kang et al., SOI conference, 2006*

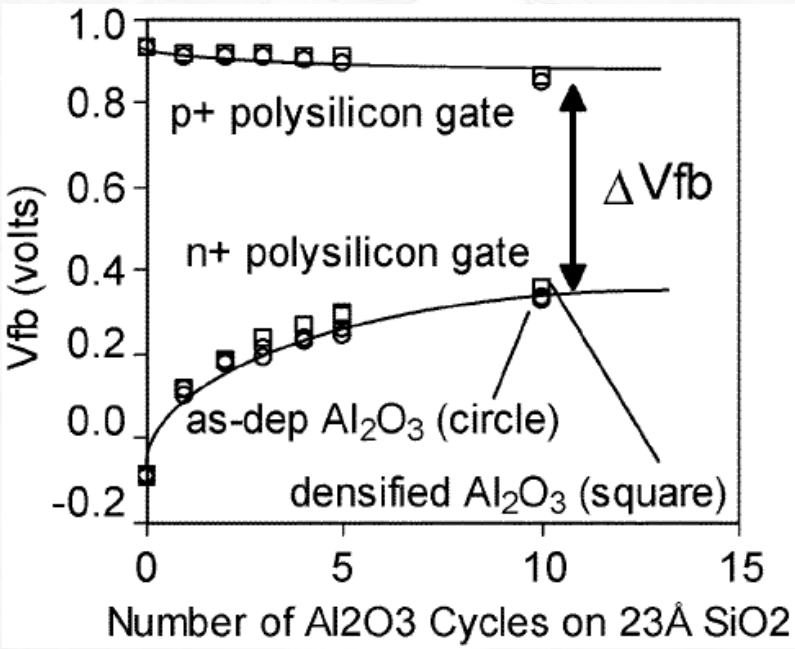
Above papers are listed as an example only

Is there a pinning at poly/HfO_2 interface?



K. Shiraishi et al., SISPAD 06





C Hobbs et al., TED 04

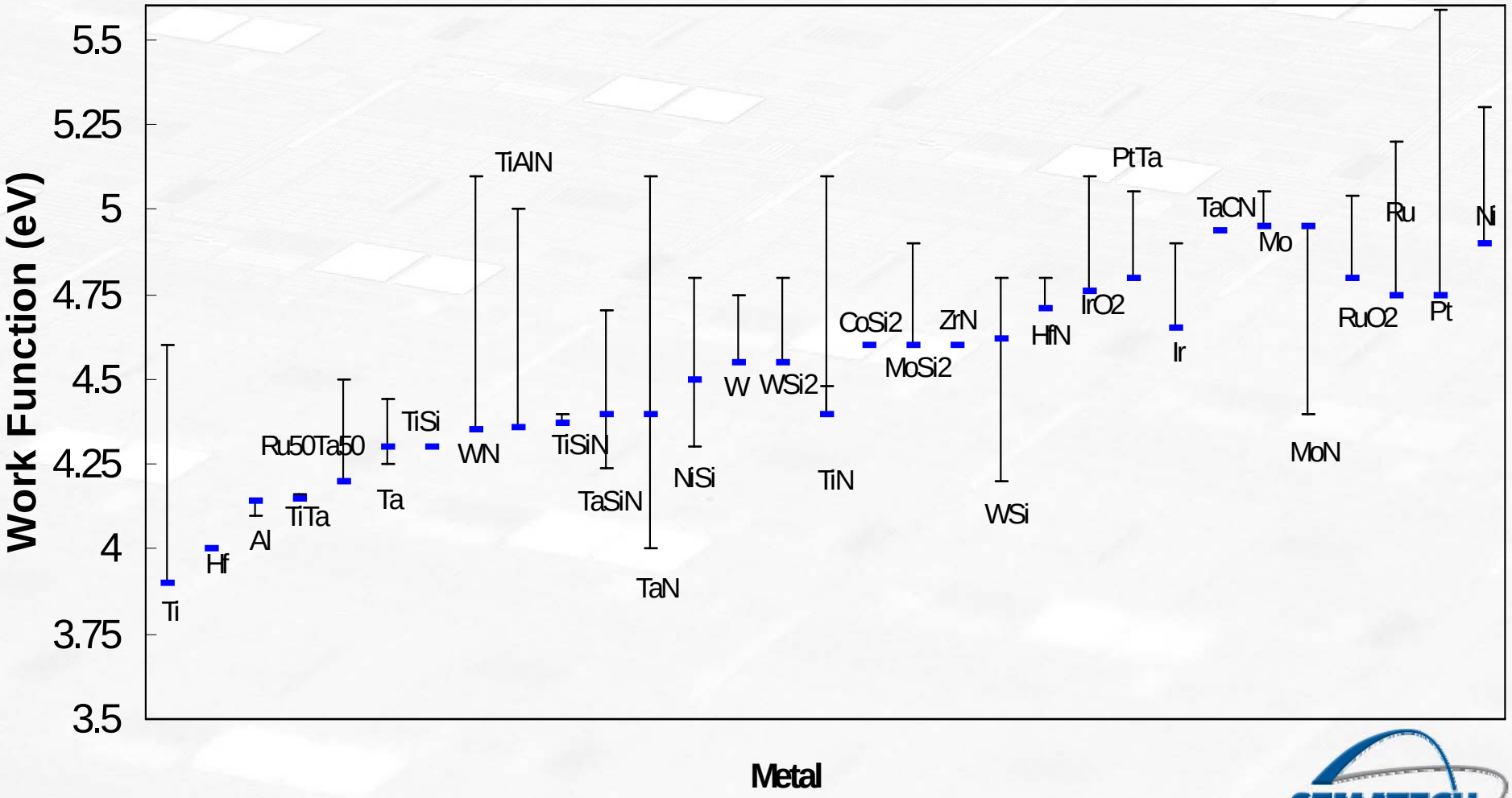
- Accuracy of EWF extraction is limited, but EWF of polysilicon is no longer controlled by E_F of Si.
- Once polysilicon is fully silicided, the discrepancy between n,p poly is minimized.
- Interface configuration determines the EWF of gate stack system.

Case 2: Polysilicon gate vs Metal gate

- Polysilicon gate and fully silicided gate works drained a majority of R&D resources and industry is moving towards dual workfunction metal gate.
  - Open communication for the cons and pros of various approaches could have saved hundreds million dollars
    - Need to encourage people to publish more about the problems as well as achievements
  - Need to focus on fundamental problems from the beginning
    - Polygate: EOT control, Vth control, reliability
    - FUSI: pattern dependence, yield challenge
    - Metal gate: problems at short channel device processing
  - Should be open minded for the possible change that cannot be avoided.

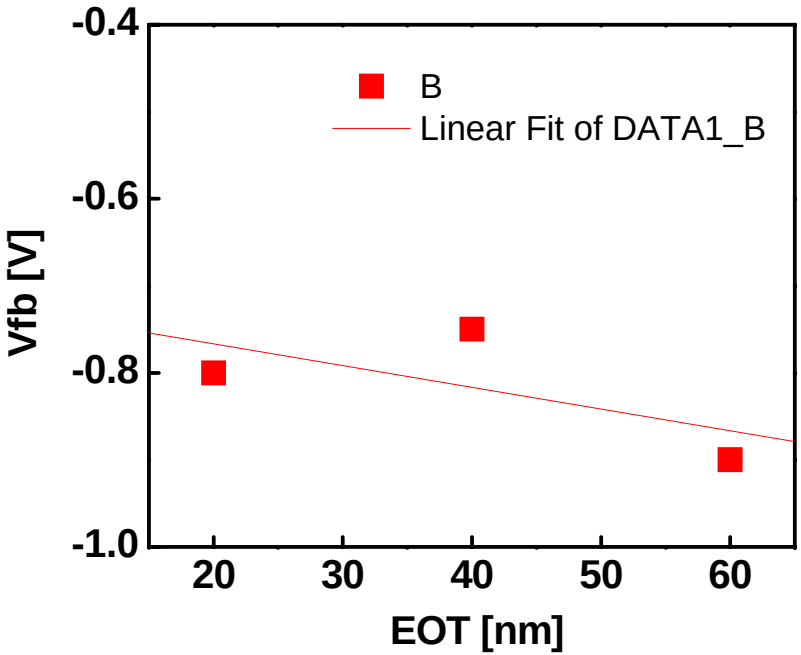
Case 3: EWF measurement and its control

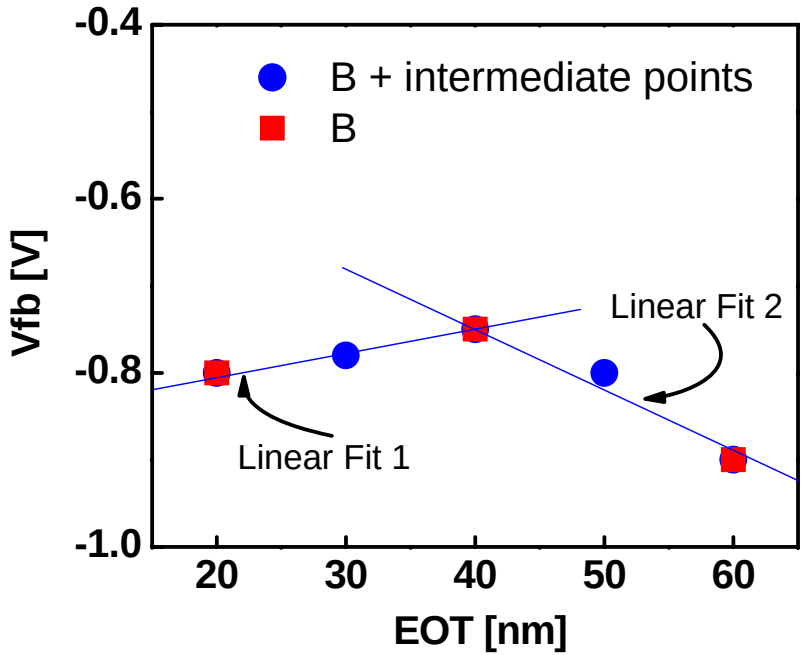
Large Discrepancy in Reported Values for Work Function of Similar Metals by Different groups



P. Majhi et al, ICICDT 2005

Scattered EWF results in the literature is partly due to the inaccurate EWF extraction method

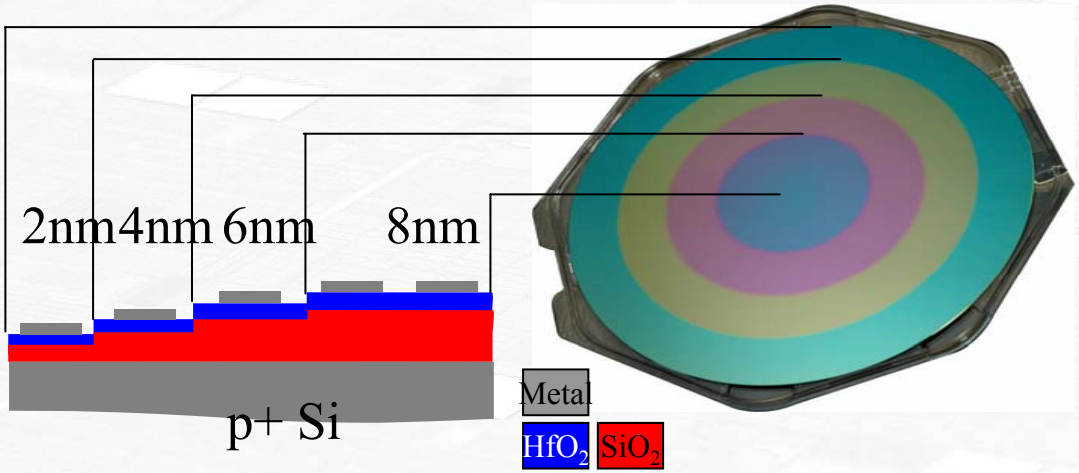




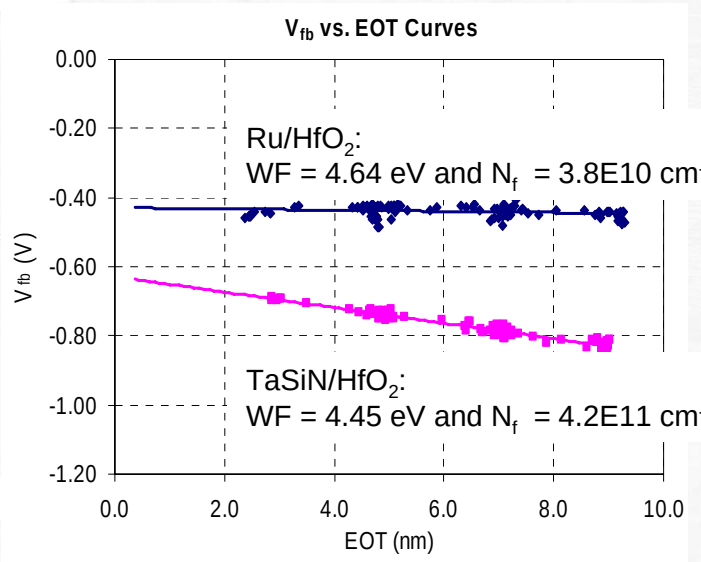
- Workfunction is a term that has a traditional physical meaning.
- Effective workfunction is defined as a loose terminology for the characteristics of electrode related to device threshold voltage.

Terraced oxide for accurate EWF extraction

- **C-V method: (terraced oxide structures)**

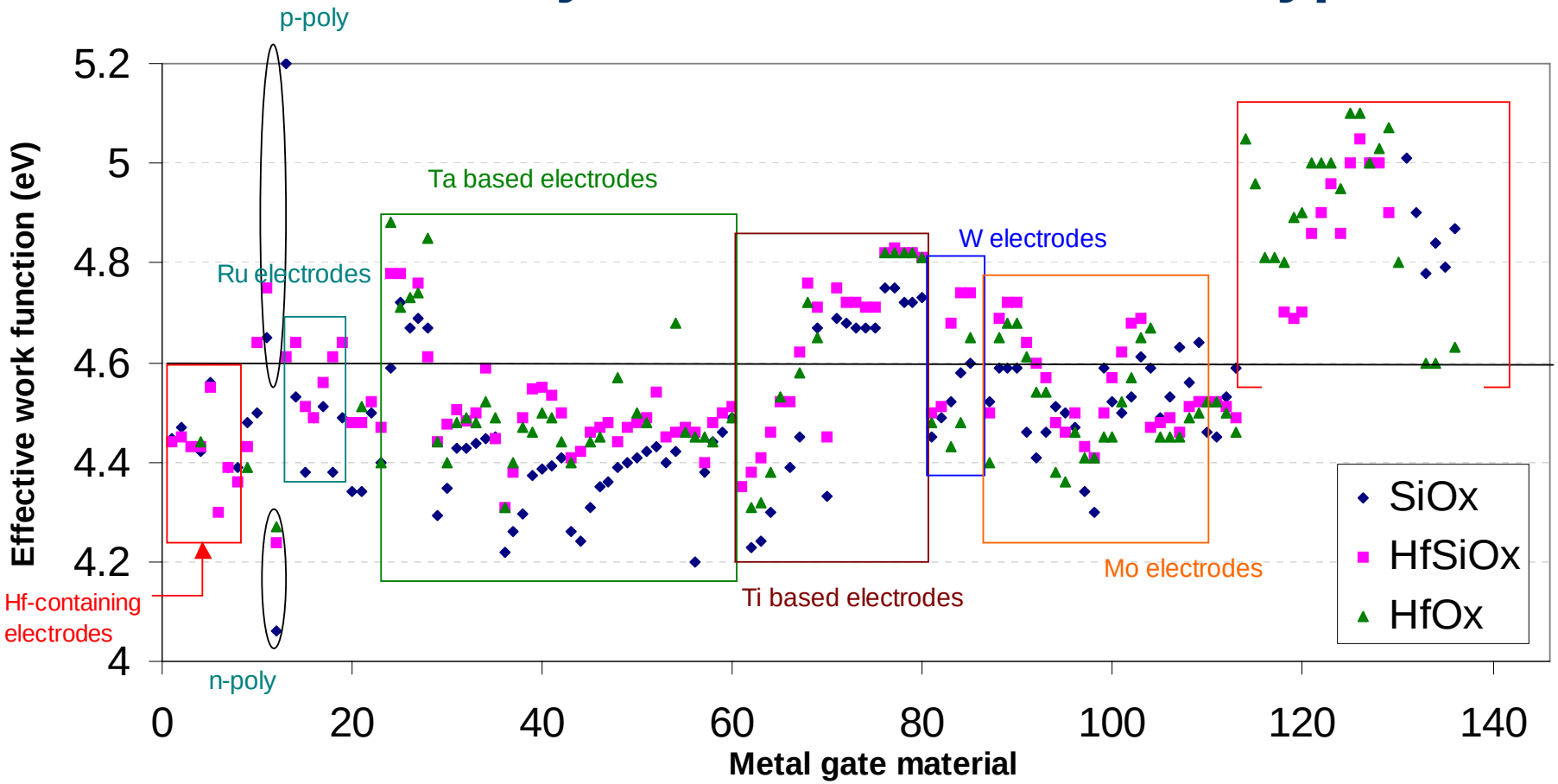


G.Brown et al., SISC 2004



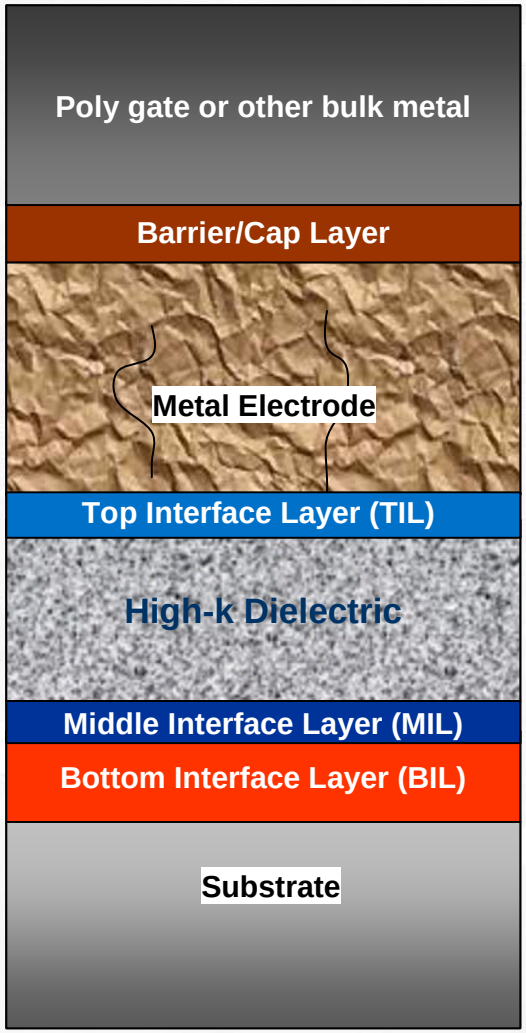
- **Effective work function extraction on:**
  - **SiO_2: varied oxide thickness from wet etch of 10nm SiO_2.**
    - **Minimize variation in Qf wafer to wafer with single SiO_2/Si interface.**
  - **High-K: Deposit thin fixed high-K thickness (3nm) on terraced oxide**
    - **Minimize bulk charge influence in high-K, controlled SiO_2 BI quality**

EWF Summary: Metal Gate Material Types



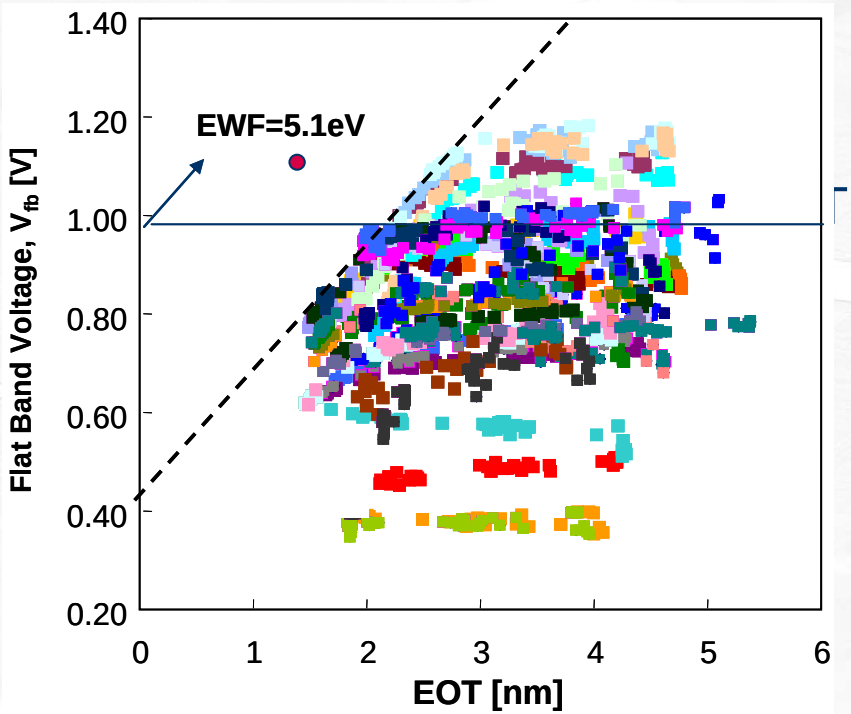
- EWF of metal electrode is affected by many other factors such as deposition process, composition of alloy, crystalline structure, impurity concentration, interaction with underlying dielectric and capping electrode, heat cycle and etc.

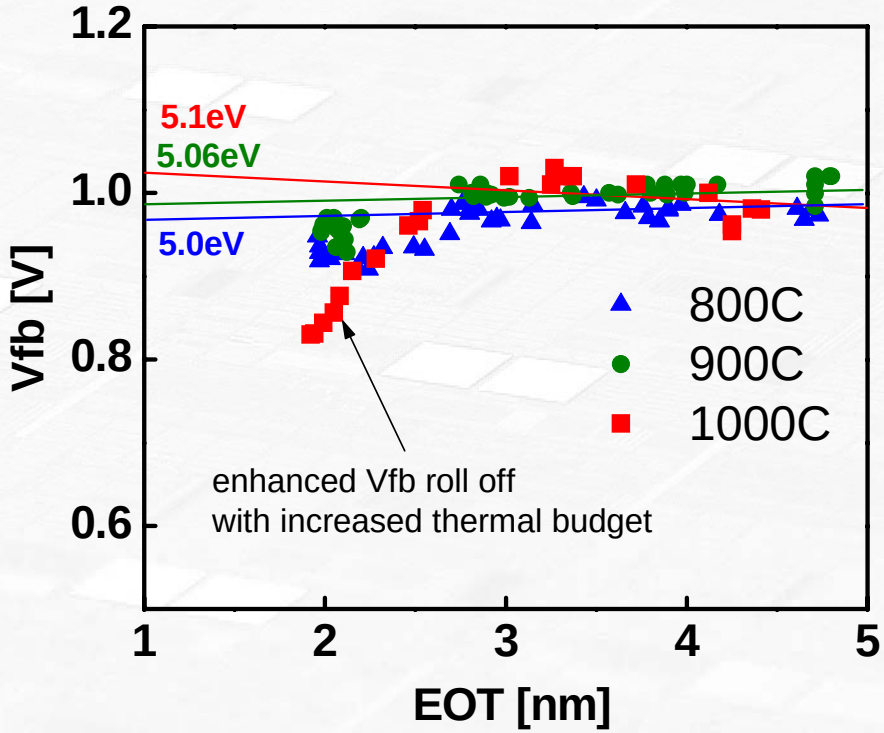
Factors affecting the EWF of electrode



- Dopant, heat cycle for activation
- Diffusion barrier for both poly gate and metal layer, intermixing
- Composition, Crystallinity, Grain orientation, Thickness, Impurities and Oxygen concentration
- Dipole formation, Diffusion barrier, Intermixing
- Composition, Impurities, Bulk charges, T_{phys} Crystalline orientation, Oxygen concentration
- Interface coordination, dipole formation
- Interface states, Oxygen concentration, T_{phys}
- Bandgap change, Strain effect

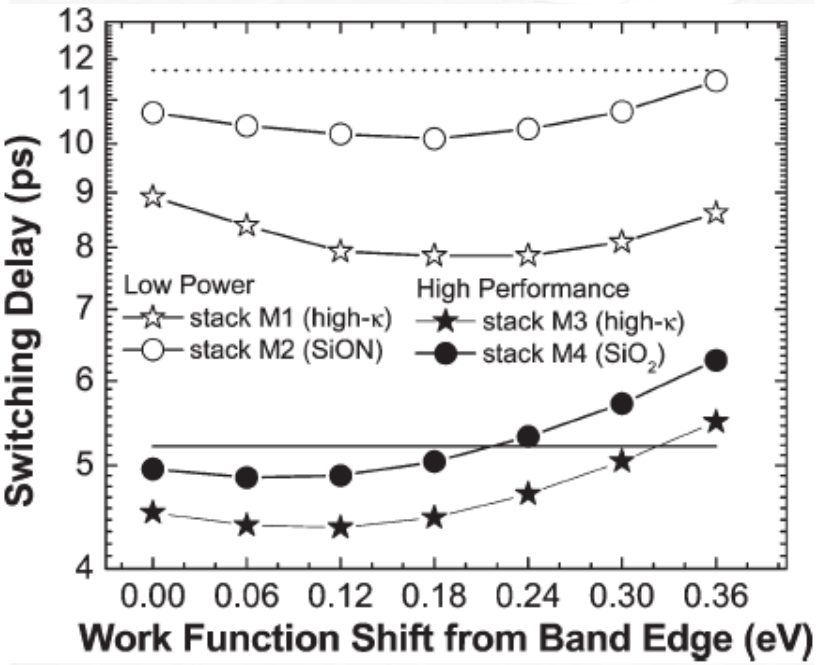
Extrinsic limitation on EWF control



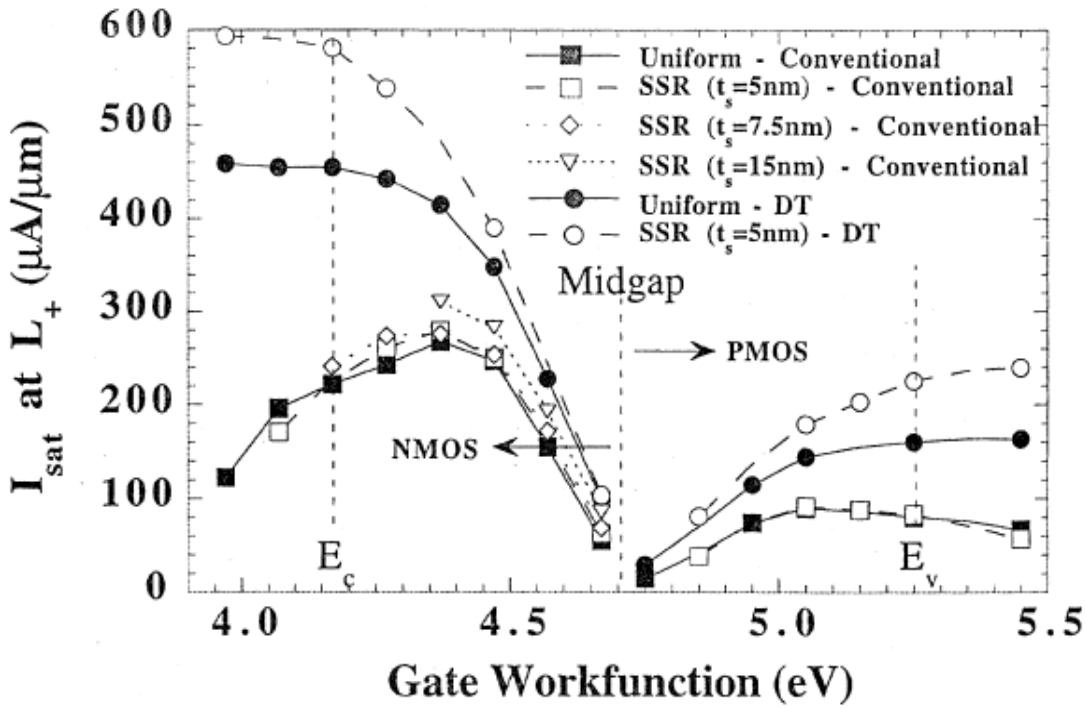


- After high temperature processing, V_{fb} rolls off at thin EOT region for for high EWF metals.
- EWF extraction at low EOT region may look like Fermi-level pinning.
- However, with a novel passivation process, this problem can be minimized.

Target for metal electrode development



A.Kumar et al., TED, 2006



I. De et al., SSE, 2000

Channel doping and EOT are adjusted.
HP target is <0.1eV off from Bandedge
LP target is ~0.2eV off from Bandedge

EOT is not adjusted/ QM effect included.
EWF <0.1eV off from Bandedge is preferred

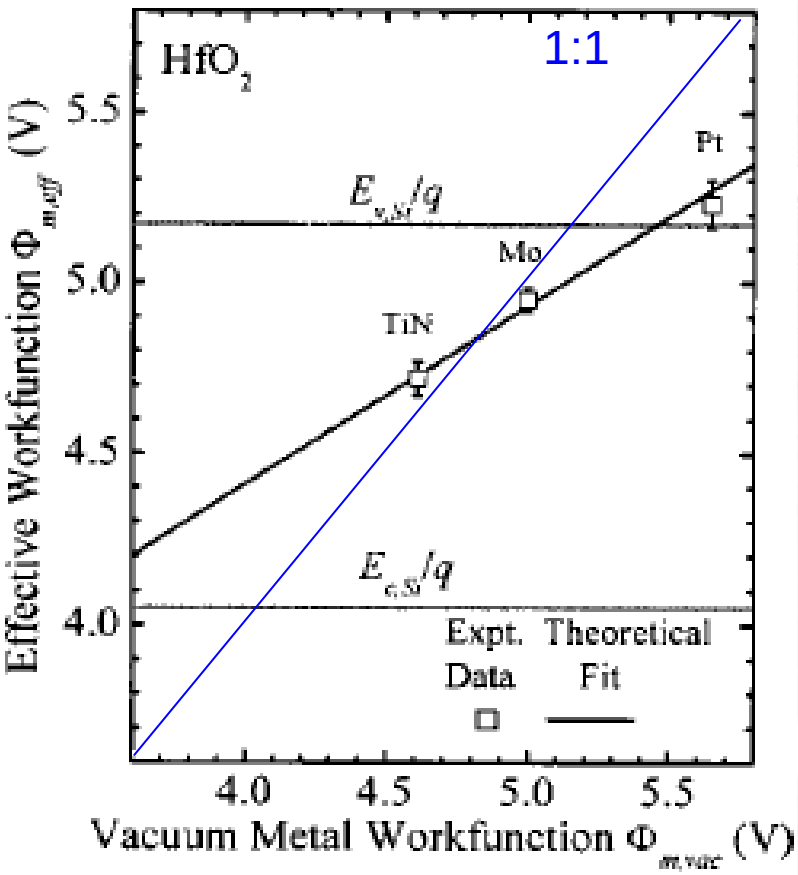
- To control the short channel effect, bandedge EWF is still preferred.

Case 3: EWF measurement and its control

- This case also emphasize the importance of characterization methods and the study at the target range
  - The importance of having a right tool cannot be emphasized more
    - Are we using right methods for Ge or III-V devices?
      - How we are handling thermal generation component in Ge or pinning vs trapping factors in III-V devices?
  - Basic aspects of metal electrode have not be studied much yet
    - Electrode grain, stress, and EWF correlation
    - Impurity effect on EWF (oxygen, carbon etc)

Case 4: Fermi level pinning – a misnomer?

Metal induced gap states (MIGS) model:



Yeo et al., *Journal of Applied Physics*, vol. 92, pp. 7266-7271, 2002

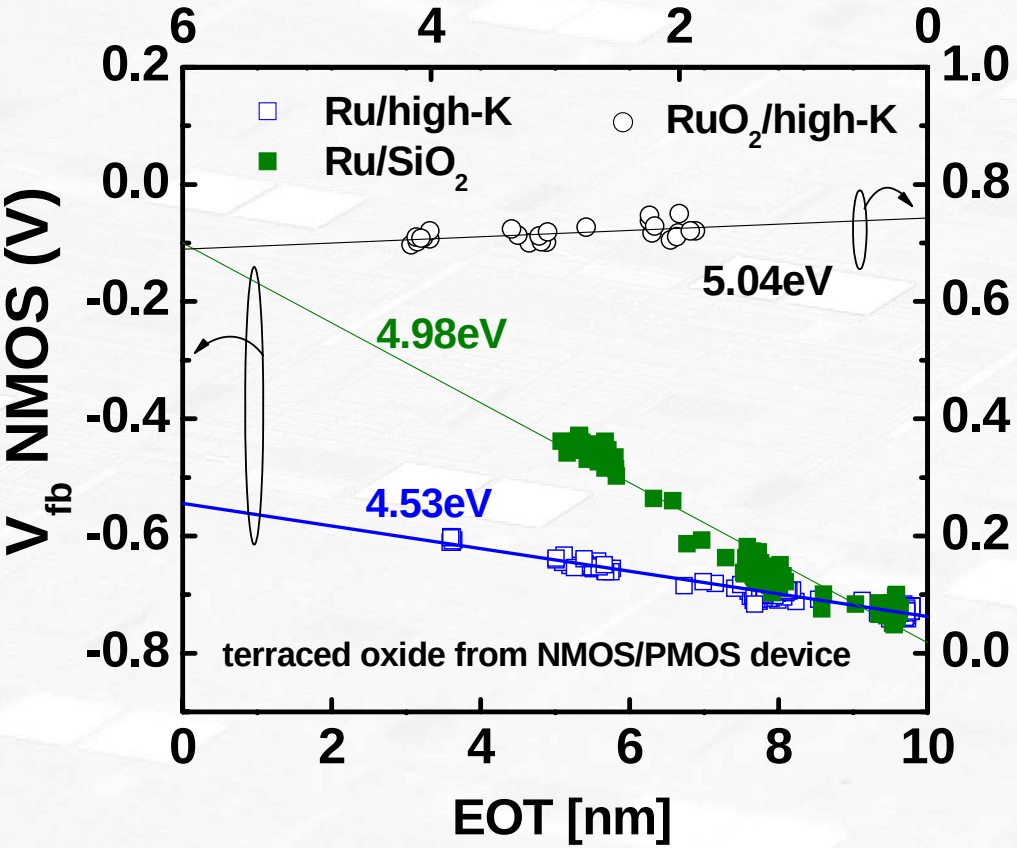
- Fermi-level pinning at metal/high-k interface limit the span of metal EWF on high-k dielectric

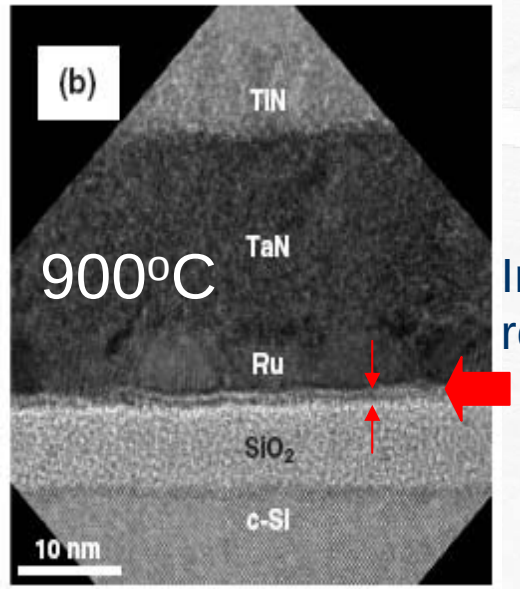
$$\Phi_{m,\mathrm{eff}} = \Phi_{\mathrm{CNL},d} + S(\Phi_{m,\mathrm{vac}} - \Phi_{\mathrm{CNL},d})$$

- Metal induce virtual states in the dielectric; interfacial charge transfer will shift the metal Ef towards the charge neutrality level (CNL)
- Metals with EWF higher/lower than Si Ec, Ev are needed to achieve band edge EWF

- **EWF measurement in this work is dependent on the dielectric system**

Addressing “Fermi-level pinning” in metal gates

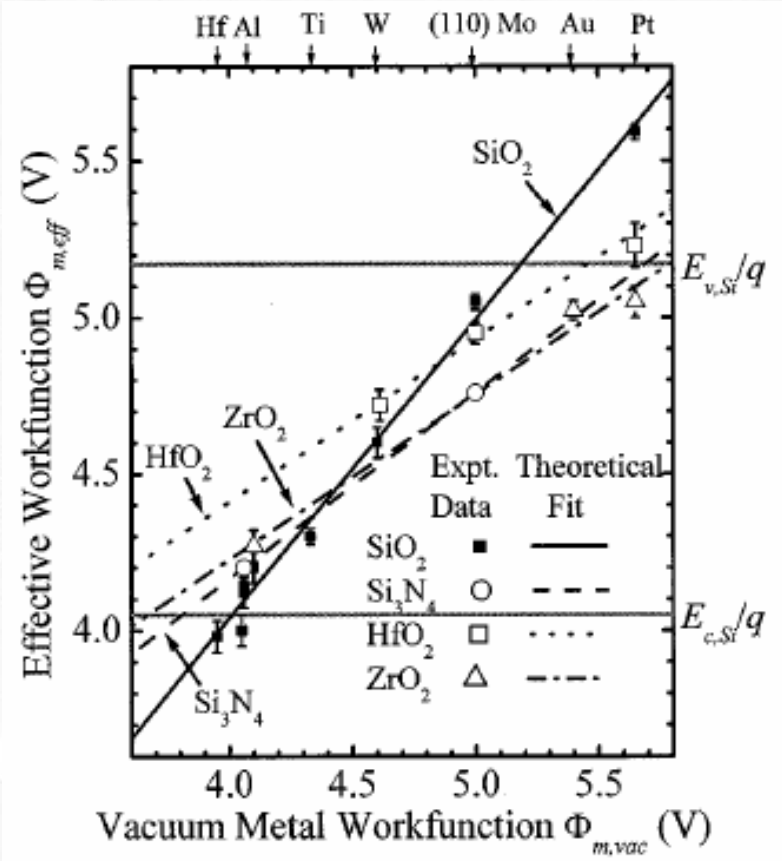




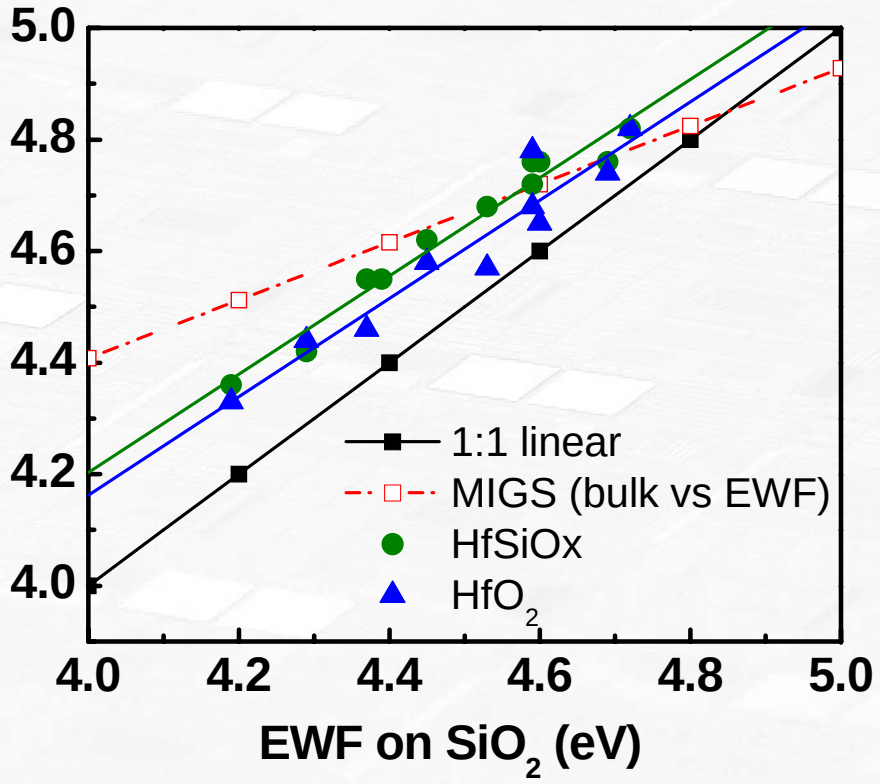
Interfacial reaction

- In many case, EWF change is due to extrinsic factors such as;
  - Compositional changes from interdiffusion
  - Interfacial reaction forming oxide [Alshareef, Thin solid films 2006]

EWF trend line for terraced oxide

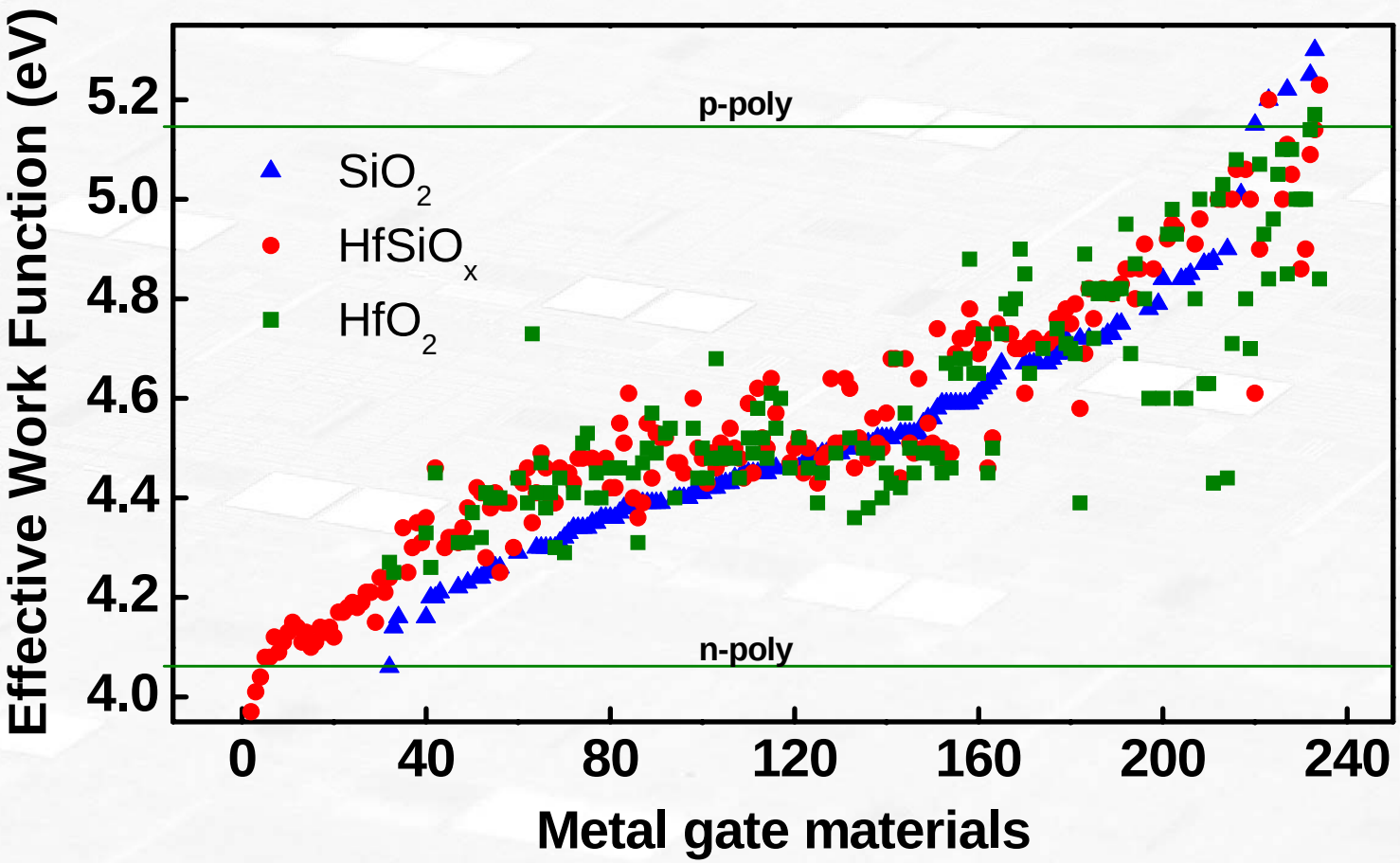


Y.Yeo et al., ELD 2002



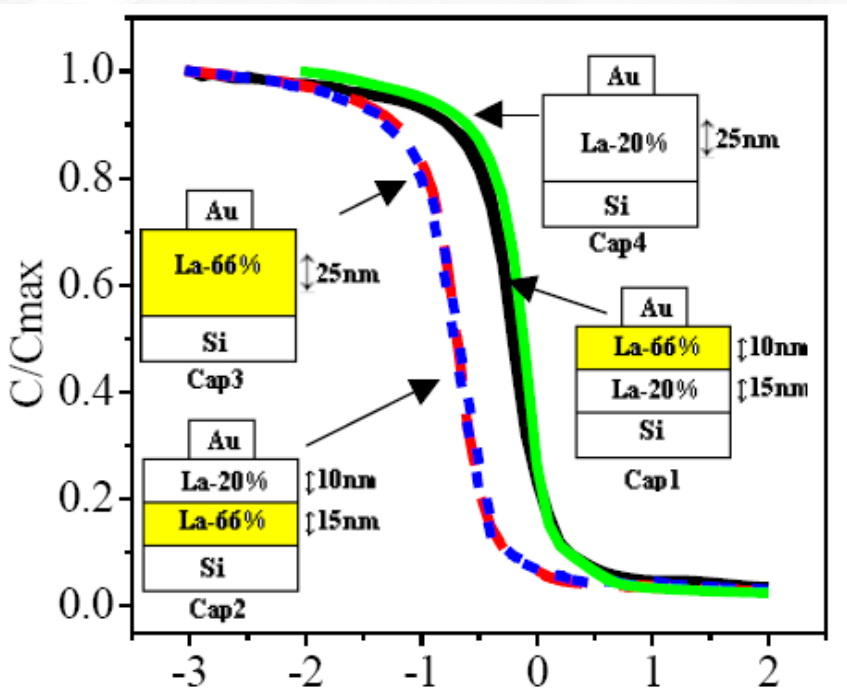
- Thermally stable electrodes exhibit parallel trend line to ideal 1:1
  > EWF is not limited by MIGS trend line

EWF of Electrode materials studied at SEMATECH



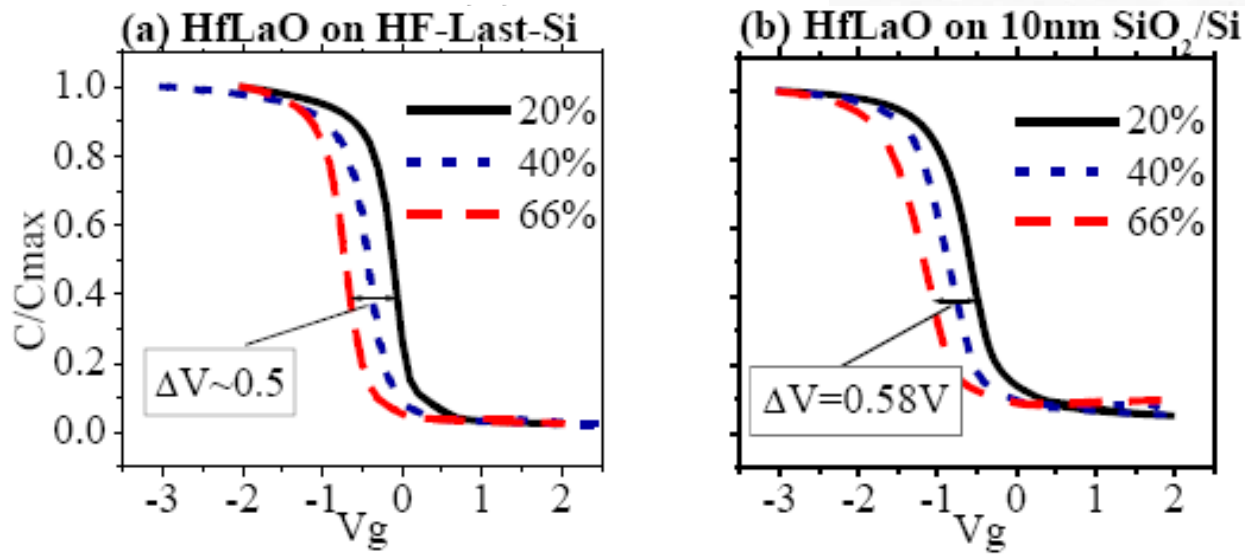
- All the data are collected after heat cycle ≥1000°C, 5sec anneal.
- For accurate EWF assessment, terraced oxide structure is used.
- For more details, please refer P.Majhi et al, ICICDT, 2005.

Internal dipole determines the Vfb shift

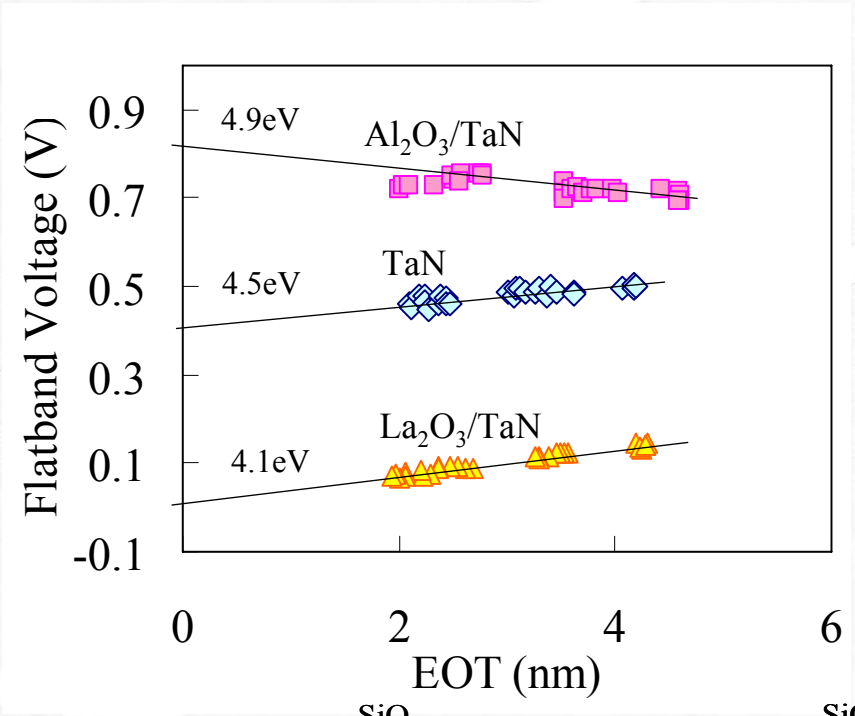


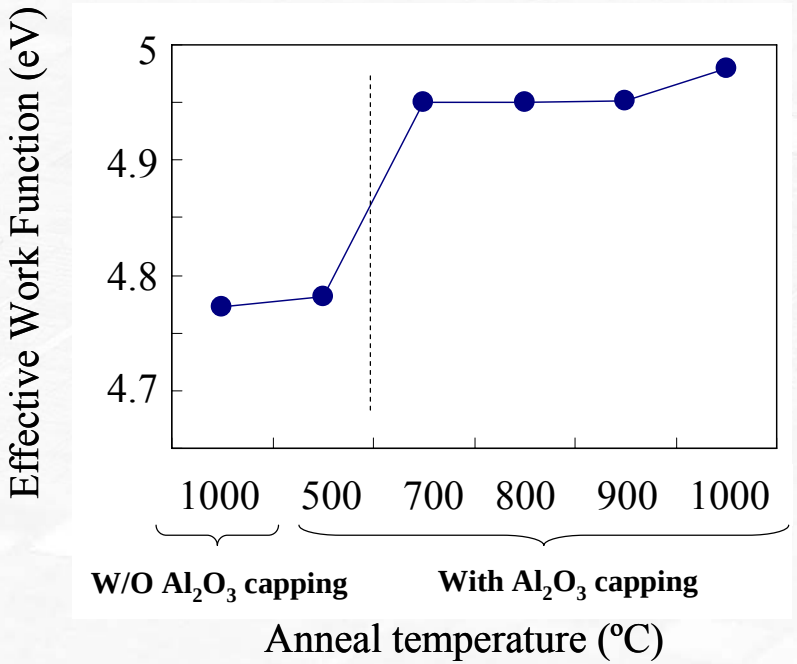
- Final Vfb is determined by the composition at bottom of the high-k layer.
- Final Vfb is not related to the interface to Si (neither Dit, nor charges at in interface)
- Internal dipole is responsible for this phenomenon

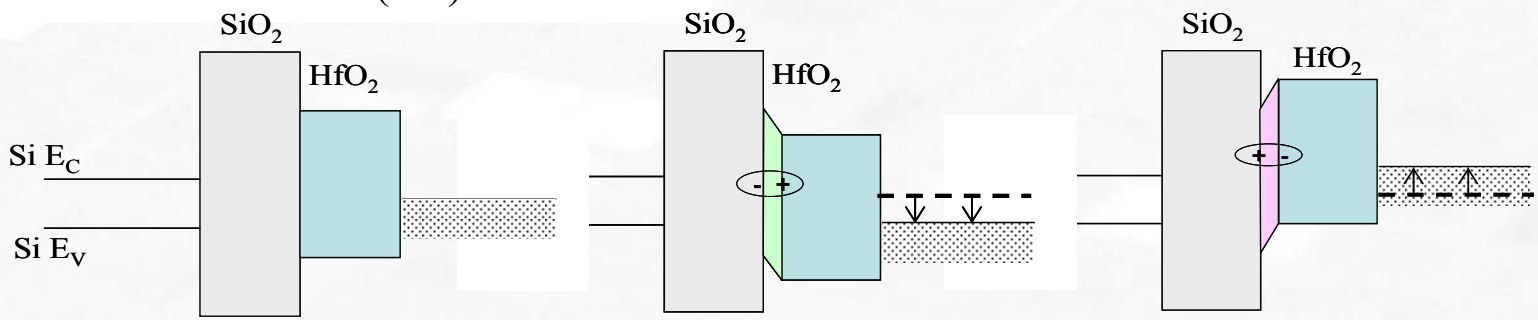
Y.Yamamoto et al., SSDM, 2006



Unified dipole model: Internal dipoles control the EWF of metal/high-k system







+ΔEWF

-ΔEWF

H.Alsahreef et al., VLSI, 2006
R. Harris et al., IEDM 2006

Case 4: Fermi level pinning – a misnomer?

- There were enough evidences that Fermi level pinning is not the right concept because EWF of metal electrode is influenced by many unknown factors, but not bound to specific defect level.
  - What about the Fermi level pinning at GaAs?
  - Need to find a way to cross check the major concepts even when it is so obvious.

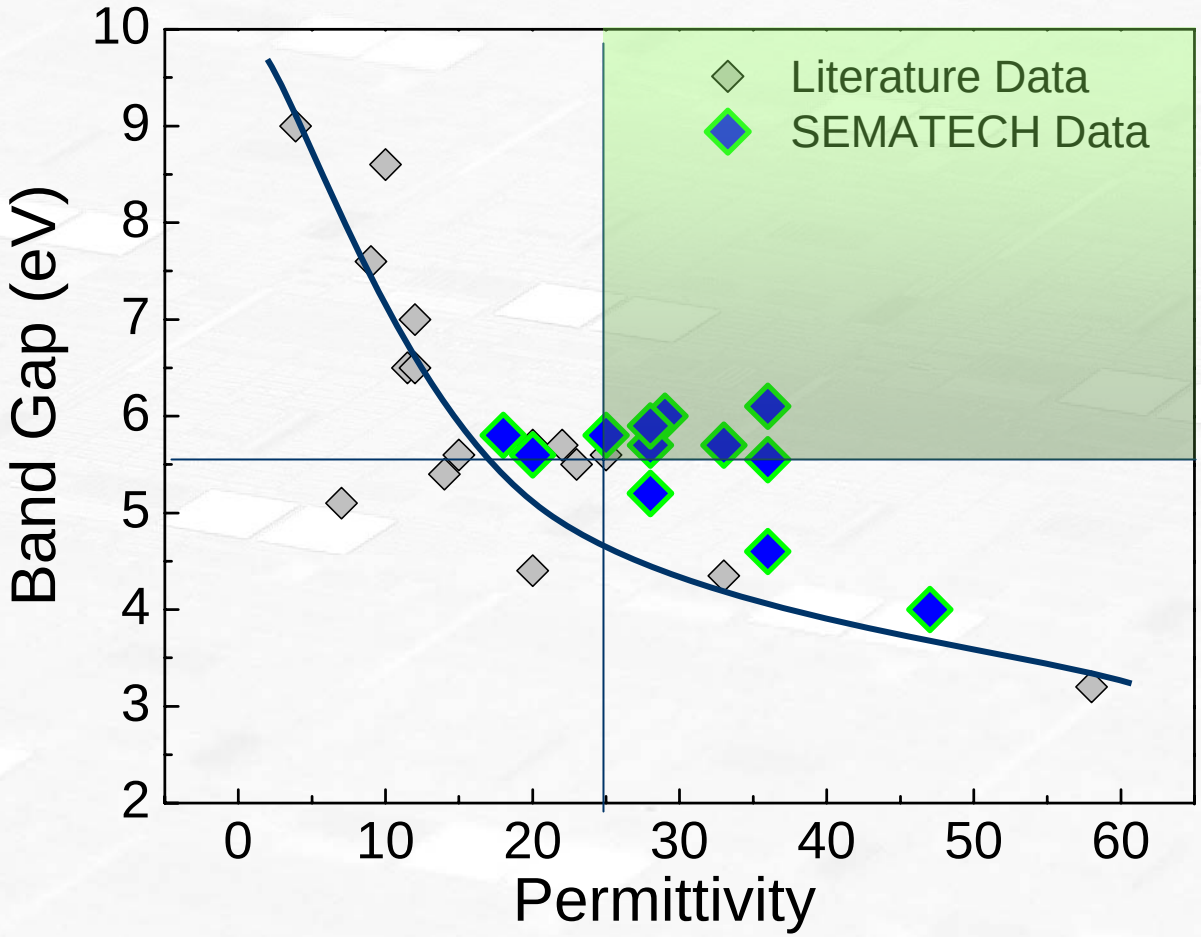
Outline

- Intro. to SEMATECH, FEP division
- Future CMOS technology
- Review of Alt. Gate Stack Research
  - Case 1: Intrinsic problem of high-k dielectric
  - Case 2: Poly silicon gate vs metal gate
  - Case 3: EWF measurement
  - Case 4: Fermi level pinning – a misnomer?
- Summary

Challenges in the Gate Stack Technology for Future Semiconductor Devices

- Targets for gate stack technology
  - Need 5-7Å EOT with low Dit
  - Medium-k material (ε<70, E_g>5eV) to avoid fringing field effect and high leakage current
  - 22nm node may require a low temperature processing < 750°C combining laser anneal, metal S/D
  - Selective epi process for dual channel application
- Application for novel devices
  - Non-planar device
    - Relaxed target, 32nm node technology can be implemented
  - Novel devices with super steep swing

High-k dielectric materials and its bandgap



- SEMATECH data is obtained from alloyed high-k dielectrics.
- Only a few materials meet the requirement of ε>25 (and Eg>5.5eV).
- Can we obtain same ε at amorphous state?

Current focus of SEMATECH AGS program

- Dual metal/dual high-k CMOS baseline
  - Device performance and reliability modeling
  - Compatibility with novel activation processes
  - Strain engineering of metal/high-k devices
- Higher-k material screening for 5Å EOT
- Interface study for MOSFETs with alternative channel
- Selective Epi process for MOSFETs with alternative channel
- Applications of metal/high-k stack
  - Charge trapping memory devices
  - MIM capacitor
  - Novel devices

Thanks!